A Novel FPGA Architecture using Memristor-Transistor Hybrid Approach

M.Hassan Aslam, Umer Farooq
Department of Electrical Engineering
COMSATS IIT
Lahore
Pakistan
{mhassanaslam, umerfarooq}@ciitlahore.edu.pk

ABSTRACT: *This work focuses on the design of a novel FPGA architecture based on memristor-transistor hybrid approach. A lot of research has been carried out in the field of FPGA that has focused on decreasing the size and power consumption of FPGAs. However, still FPGAs are larger in area, slower in speed and more power consuming. In this work, basic building blocks like MUX, NOR gate, D flip flop, NOT gate and buffer are designed and implemented using memristor-transistor hybrid approach. These basic building blocks are combined to form Configurable Logic Blocks (CLBs), Switch Boxes (SBs) and Connection Boxes (CBs) of FPGA. Proposed hybrid basic building blocks of FPGA are smaller in size and lower in power consumption as compared to the conventional transistor-only building blocks. For experimental purpose, first we compare the area and power of conventional and proposed basic building blocks and achieve the average area and power efficiency of 30% and 60% respectively. Similarly, the area gain of a 2 input single tile based on proposed basic building block is 39%. Then, we also explore the overall area of memristortransistor hybrid FPGA architecture for sixteen largest MCNC benchmarks and present the results.*

Keywords: Memristor, Hybrid FPGA, Simulation, Design Flow

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1. Introduction

LEON CHUA discovered a fourth fundamental circuit element in 1971. This two terminal device is called memristor. Memristor provides the missing relationship between flux linkage and charge [1]. He proved that already existing elements can not duplicate the behavior of memristor, as shown in Figure 1a. Memristor changes its resistance with the polarity and magnitude of voltage applied across its terminals. Furthermore, it also remembers the value of voltage until the voltage is reapplied, whether that happens a year later [2]. Memristor was a brilliant but under-appreciated discovery till 2007. It got researchers' attention when in 2008 Hewlett-Packard (HP) labs explored physical memristor [2]. It has been established that memristor is smaller in size and low power consuming device. Memristor can be used in the construction of logic gates, memories, and programmable switches. It can also be used in the design of reconfigurable architectures [2].

The computational demands of digital systems continue to grow, and effective yet simple techniques are becoming increasingly significant to minimize area, power, and energy consumption. Whereas memristors are smaller in area, two order of magnitude

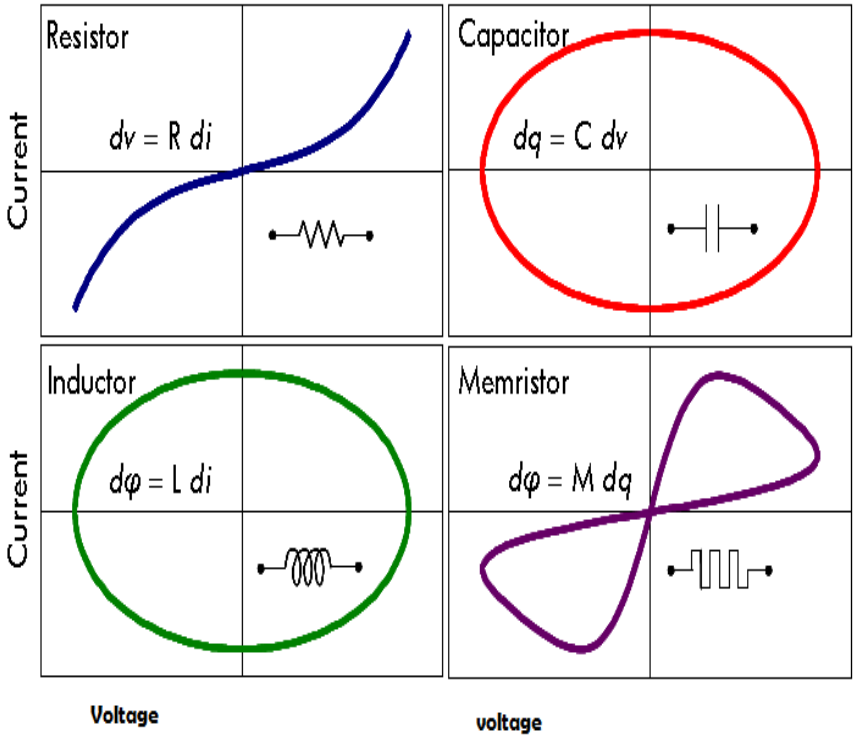
efficient than transistors, and have the switching capability (speeds) of only a few nano seconds [3] [4]. So, memristor can be a substitution of transistor [3] [5].

Field Programmable Gate Arrays (FPGAs) were introduced in 1985. Initially, FPGAs were only used as glue logic but now these prefabricated devices can be programmed for any kind of digital circuit. FPGAs have numerous advantages over Application-Specific Integrated Circuits (ASICs). For instance, standard cell ASICs normally take months for fabrication and have a high Non-Recurring Engineering (NRE) cost of first device [6]. On the other hand, FPGAs can be configured instantly having no NRE cost. The reconfigurability of an FPGA is achieved at the cost of area, speed, and power consumption. FPGA consumes approximately 20 to 35 times more area, 10 times more power, and is 3 to 4 times slower in speed than a standard cell ASIC [6].

FPGAs are renowned devices in digital system designing and prototyping. Its reconfiguration is achieved through multiplexers, switches, pass transistors, D flip flops and SRAMs. It is explored that 90% of the area and 85% of the power consumption in FPGA is due to reconfiguration [6]. Conventional FPGAs are constructed using combinationof basic building blocks, which are further made up of transistors. For example, six transistors are used for SRAM, four transistors are required for 2x1 MUX, and two for buffer. Now if the area of each building block is reduced by using some component other than transistor, it will have a dramatic impact on the overall area and power consumption of FPGA.

This journal paper is the extended version of [7]. In this work, we design and simulate basic building blocks of FPGA based on memristor-transistor hybrid approach. On the bases of these building blocks a novel FPGA architecture is proposed, which leads towards a much smaller and efficient FPGA architecture with less power consumption. Area of complete memristor-transistor FPGA architecture is also explored with the help of a specially customized Computer Aided Design (CAD) flow which is based on [8]. For experimentation, we place and route sixteen largest MCNC benchmarks [9] on the proposed architecture using the aforementioned CAD flow.

The rest of the paper is organized as follows: section II reviews the recent research work on memristor and its integration with Complementary Metal-Oxide Semiconductor (CMOS). The proposed circuit designs of basic building blocks of FPGA using memristor-transistor hybrid approach are presented in section III. In section IV, comprehensive results of circuit simulations are discussed followed by the area results of complete FPGA architecture. Finally, this work is concluded and future prospects are presented in section V.



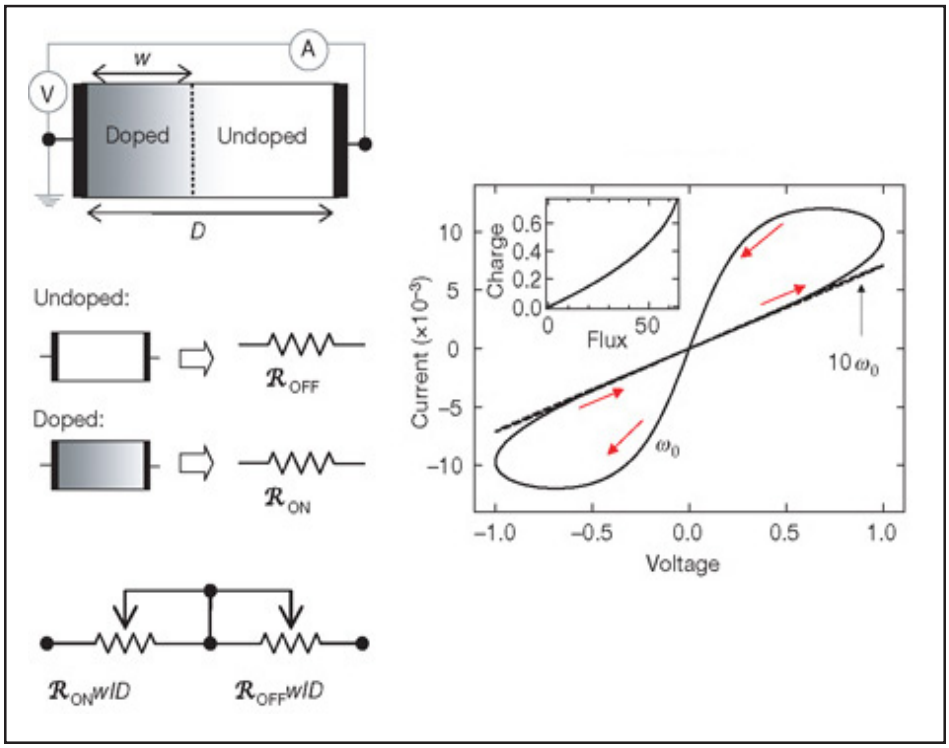


Figure 1. (a) I-V Characteristics of fundamental elements; (b) Model and I-V characteristics of Hewlett-Packard (HP) memristor

2. Related Work

In last two decades, transistors have been scaled down fiercely, even exceeding Moore's law. Scaling below 20 nm in size creates intimidating challenges. These challenges become unmanageable when process technology scales below 15 nm [10]. In recent years, many technologies have been scientifically probed to find a solution.

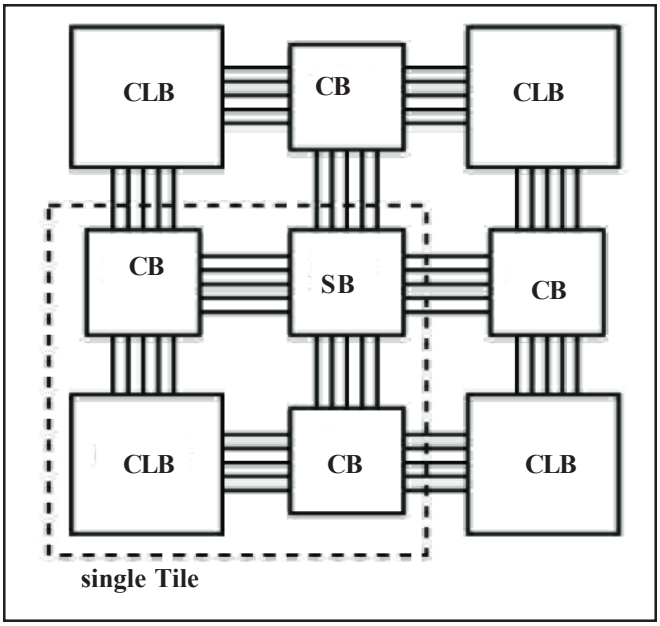
A physical memristor model has been presented by HP labs that produces a rich hysteresis loop as shown in Figure 1b. Memristance is achieved by sandwiching a thin semiconductor film between two metal plates [3]. The boundary of the doped and undoped regions varies by applying the voltages across plates, which causes the hysteresis effect. Due to this unique property, the semiconductor industry is drawn towards the use of memristor as a replacement for transistor. Memristor can be used for many other applications [11]. A flamboyant application is the use of memristors as a part of logic circuits. Memristors can be used to design and develop logic gates. Plenty of schemes have been proposed to perform logic operations using memristor i.e Memristor Ratioed Logic (MRL) [12], Memristor-Aided Logic (MAGIC) [13] and IMPLY logic [14]. Memristors can also be used as reconfigurable switches, which can be immensely helpful in designing a new architecture for FPGA [15] [16].

Integration of memristor with CMOS devices is a prevalent research domain. Combination of memristor and CMOS devices can provide 2-3 times area improvement and lowers the power consumption by 20% [17]. To replace the conventional CMOS devices, novel CMOS-memristor devices are being developed, through which significant power reduction and density improvements can be achieved. CMOS-memristor hybrid approach is fabrication compatible. HfO_2 and ZrO_2 are some of the materials being used for CMOS technology. These materials can also be used in the fabrication of memristor [18] [19].

The performance of memristor is directly linked with size, smaller the size better will be the performance of memristor [16]. One of the major advantages of memristor is its non-volatile nature. Memristor can retain its state for years without any power [2] [3]. In conjunction with all the properties stated above, the integration of memristor and CMOS devices will lead to technology breakthroughs in future nano technology era [20].

In this paper, we propose a novel memristor-transistor hybrid FPGA architecture which is compatible with current fabrication technologies. Existing work has incorporated memristors in building routing structures, or replacing some memory elements

(e.g. SRAM) with the hybrid ones [16] [17] while we have incorporated memristor in the design of basic building blocks of FPGA. These basic building blocks are area and power efficient. Using these basic building blocks, a novel memristor-transistor hybrid FPGA architecture is proposed. This novel memristor-transistor hybrid FPGA is area and power efficient. For experimentation, We have used sixteen largest MCNC benchmarks to explore the complete area of novel memristor-transistor FPGA architecture.



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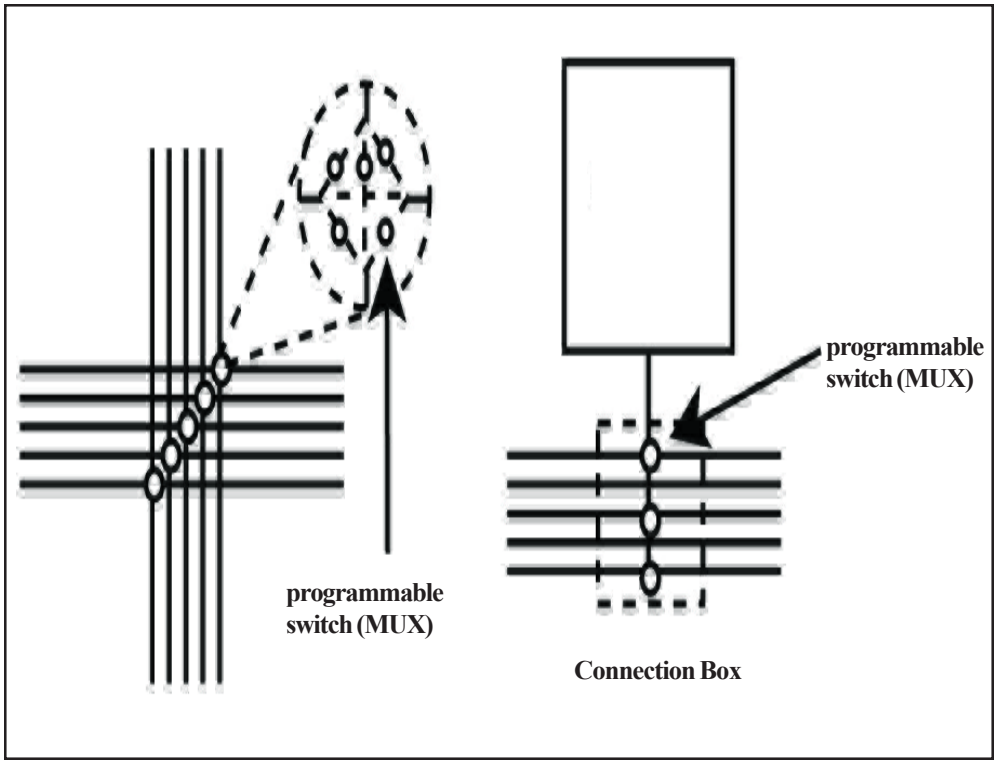


(b)

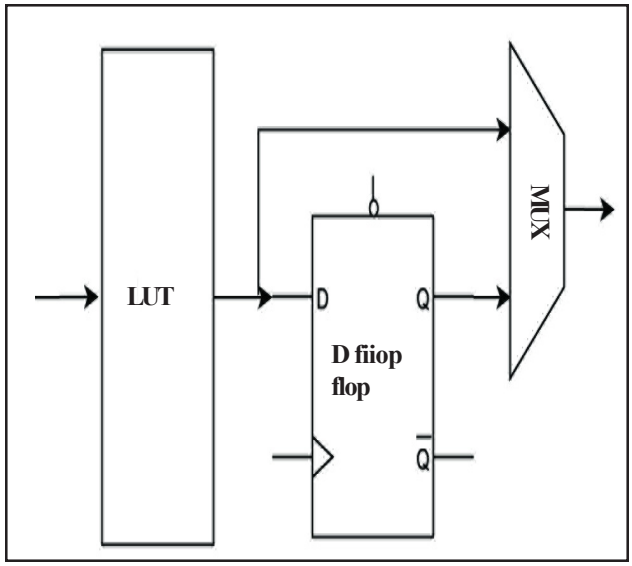
Figure 2. (a) FPGA Architecture; (b) Switch box and Connection box

3. Proposed Basic Building Blocks of FPGA

An abstract level view of an island style homogeneous FPGA is shown in Figure 2a. It can be seen from Figure 2a that blocks inside dashed box constitute single tile of an FPGA. These tiles are then replicated to build large FPGA architecture. Each tile consists of one CLB, SB, and two CBs. The CLBs are connected together through SBs and CBs to form a complete FPGA architecture. Figure 2b depicts the design of SBs and CBs based on programmable switches. Figure 3a shows internal structure of a simple CLB. As it can be seen from the figure that inside a CLB, there are Look-Up Tables (LUTs), D Flip Flops and Multiplexers (MUXs). A LUT consists of SRAMs and MUXs. The internal structure of a two input LUT is shown in Figure 3b. Thus, in order to make CLB, SB and CB, we require SRAMs, D flip flops and MUXs; which we term as the basic building blocks of FPGA. In the following part of this section, we give an overview of the proposed structure of each basic building block. Details on the design of these basic building blocks are already presented in [7].

3.1 Multiplexer 2x1

A 2x1 Multiplexer contains 4 transistors and a NOT gate. While using the memristor-transistor hybrid approach, we reduce this number to 2 transistors only. Our design incorporates 2 transistors and 2 memristors. A schematic of our multiplexer is shown in Figure 4a.



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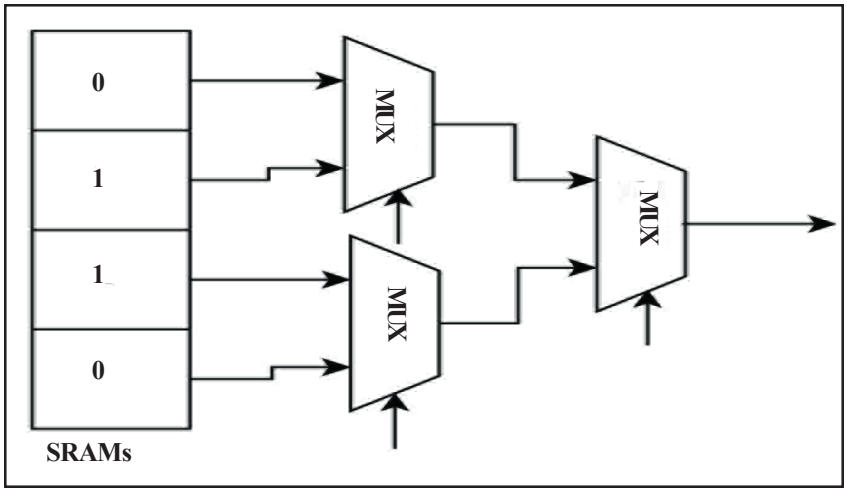

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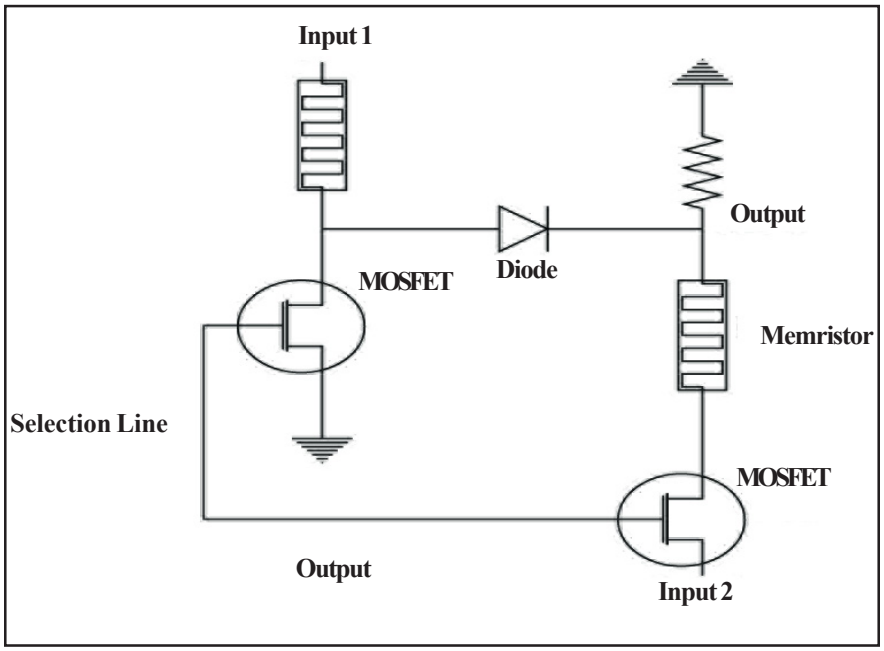
Figure 3. (a) Configurable Logic Block; (b) Look-Up Table



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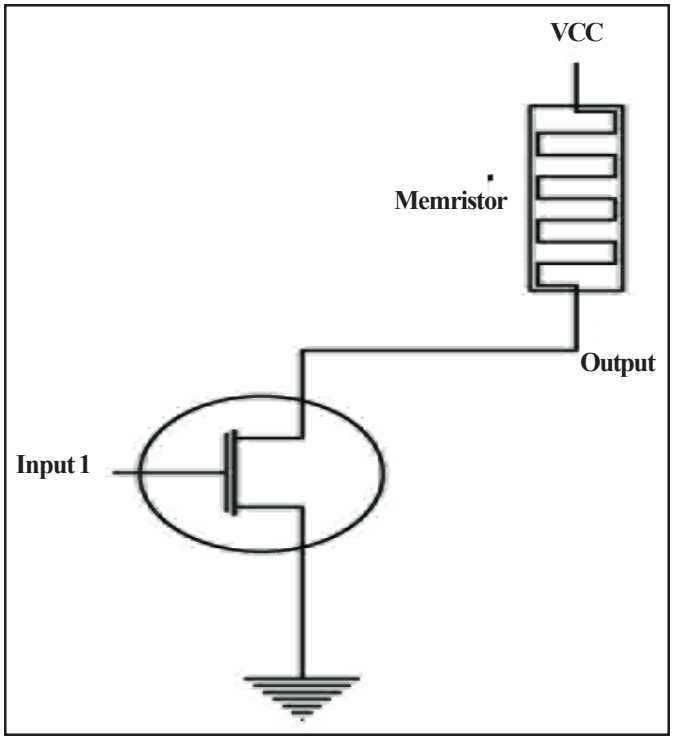

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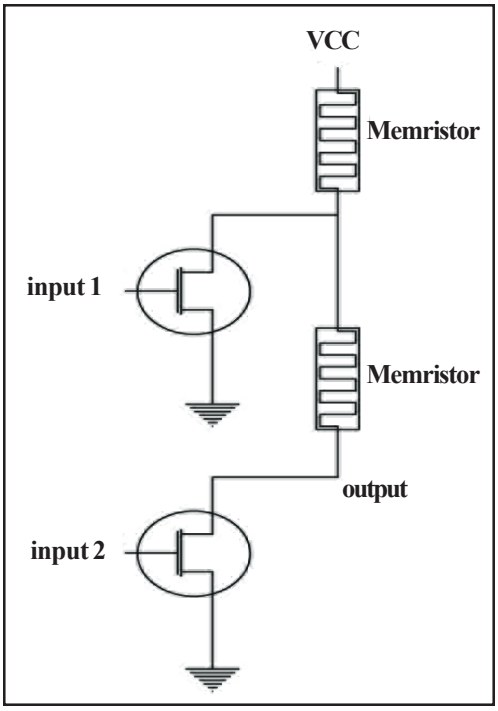
Figure 4. (a) MUX 2x1 using memristor-transistor hybrid approach; (b) NOT gate using memristor-transistor hybrid approach

3.2 NOT Gate

Conventionally, there are 2 transistors inside a NOT gate. While our design contains only one transistor and a memristor. A schematic of the NOT Gate, built using memristor-transistor hybrid approach, is shown in Figure 4b. A buffer can be constructed by connecting two of these NOT gates in series. Conventionally there are 4 transistors inside a buffer but our design contains only 2 transistors and 2 memristors.

3.3 D Flip Flop

NOR Gate is a universal gate and using this universal gate we designed D flip flop. Conventionally, a NOR gate uses 4 transistors. We designed the hybrid NOR gate with only 2 transistors and by incorporating 2 memristors. Figure 5a shows the schematic of our NOR gate built using memristor-transistor hybrid approach. We proposed a new D flip flop model by using our hybrid NOR gate as shown in Figure 5b. This basic building block is constructed using the two input NOR gate. We reduced the number of transistors to half in our proposed NOR gate. And by incorporating it in the D flip flop design, we have reduced the number of transistors in a D flip flop by 12.



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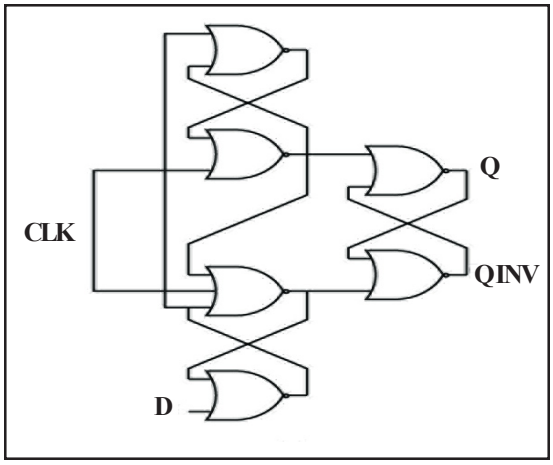

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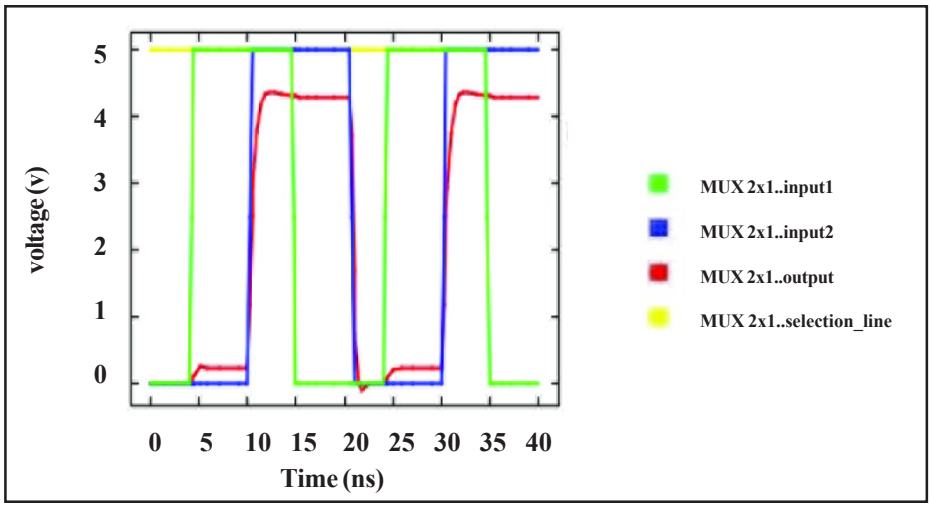
Figure 5. (a) NOR gate using memristor-transistor hybrid approach; (b) D flip flop using NOR gates

4. Experiments and Results

Results presented in this section are mainly divided into three parts. First, we present the HSPICE simulation results of basic building blocks, whose schematic diagrams are already presented in section 3. Then, the area and power consumption of

Name	Parameters	Values
R_{on}	Memristor resistance(conducting)	1 Ω
R_{off}	Memristor resistance(non-conducting)	100 Ω
R_{init}	Initial memristor resistance	5 Ω
d	Memristor film thickness	10nm

Table 1. List of Parameters for Memristor Model



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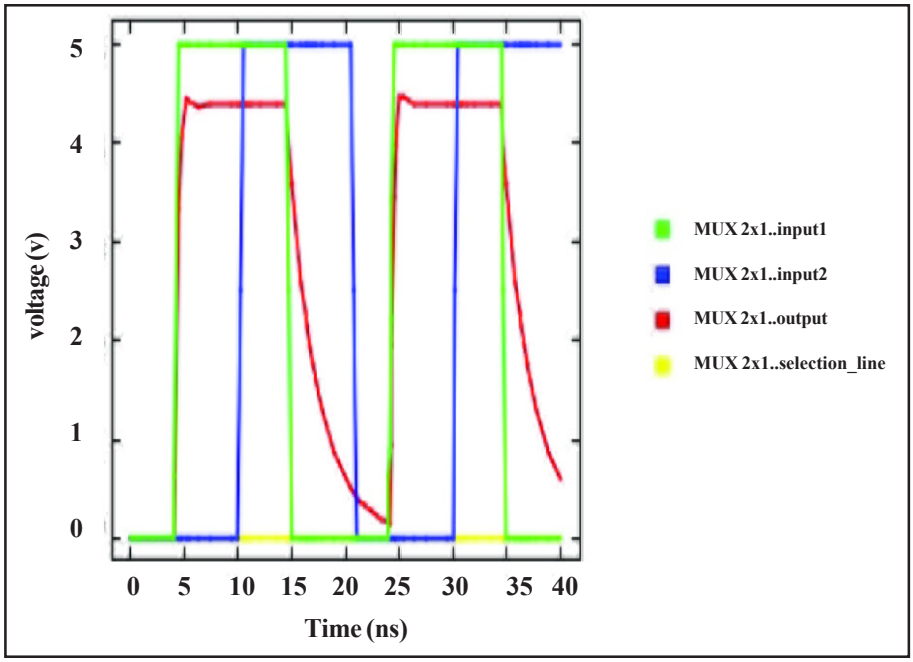

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Figure 6. (a) MUX 2x1 (selection line one); (b) MUX 2x1 (selection line zero)

memristor-transistor hybrid basic building blocks are explored and relevant results are presented. We also explored the area result of a single tile of FPGA architecture. Finally, we present comprehensive area results of memristor-transistor hybrid FPGA architecture. These results are based on the customized version of design flow presented in [8].

4.1 HSPICE Simulation Results

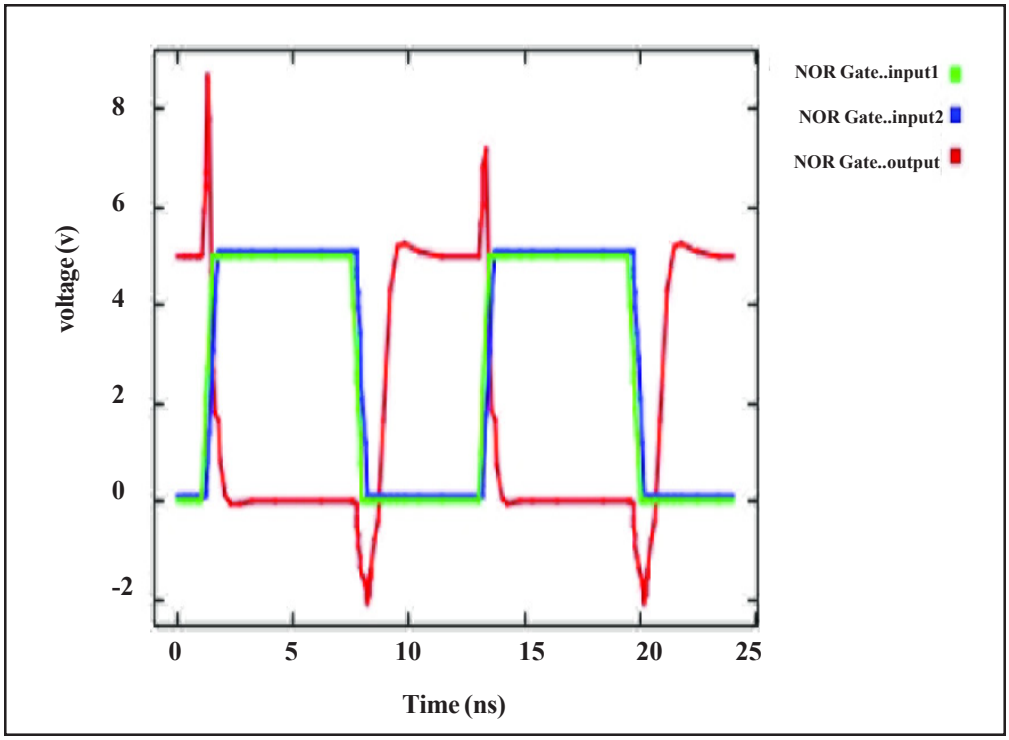
We have designed and simulated basic building blocks of FPGA using HSPICE. As no standard model exists for memristor. We have used the available memristor model specified in Table 1 [21]. First a 2x1 multiplexer was simulated as described in section 3. The applied voltages and their corresponding outputs are shown in Figure 6a and Figure 6b respectively. The output clearly shows the behavior of 2x1 MUX. The conventional 2x1 MUX requires 6 transistor. Compared to that our proposed design requires only 2 transistors, 2 memristors and 1 diode. Thereby reducing the number of transistors by 4 in a single 2x1 MUX.

NOR gate as described in section 3 was simulated. The applied inputs and corresponding outputs are shown in Figure 7a and Figure 7b respectively. This result clearly showed that proposed circuit functions like a NOR gate. D flip flop was also simulated using our custom NOR gate. D flip flop results are shown in Figure 8a and Figure 8b. Lastly, NOT gate was simulated. Inputs and corresponding outputs are shown in Figure 9a. Transistor based NOT gate consists of 2 transistors while our proposed memristor-transistor hybrid NOT gate is made up of 1 transistor and 1 memristor only. We have also simulated a buffer using two customized NOT gate. By applying a square wave to the circuit, we got the corresponding output of a buffer shown in Fig 9b by red color.

4.2 Area and power analysis of basic building blocks

In digital systems dynamic power consumption is major source of total device power consumption. Dynamic power consumption is directly linked with state transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) of basic building blocks of device under consideration. Power analysis of these designs is also performed and their average power consumption is evaluated using HSPICE. Average power of each conventional as well as hybrid building block is shown in Table 2. It is clear form the table that for all blocks, proposed hybrid approach gives better results as compared to conventional transistor-only approach. Results shown in the table indicate an average power gain of 60% for proposed building blocks compared to the conventional building blocks.

When the whole FPGA architecture is considered, millions of transistors are used to construct these basic components. For



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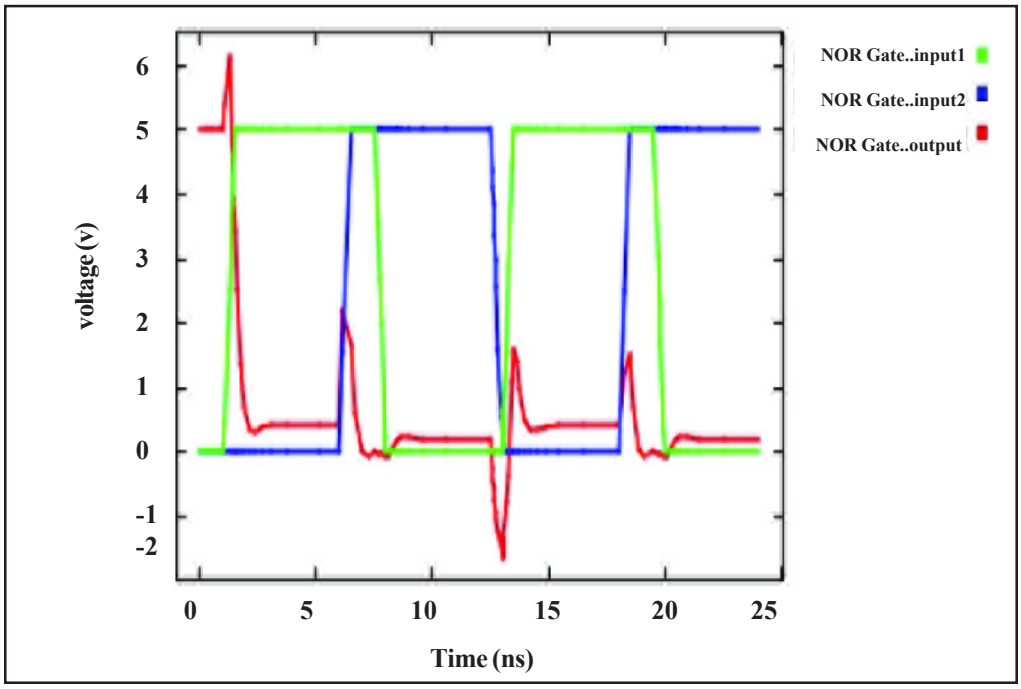

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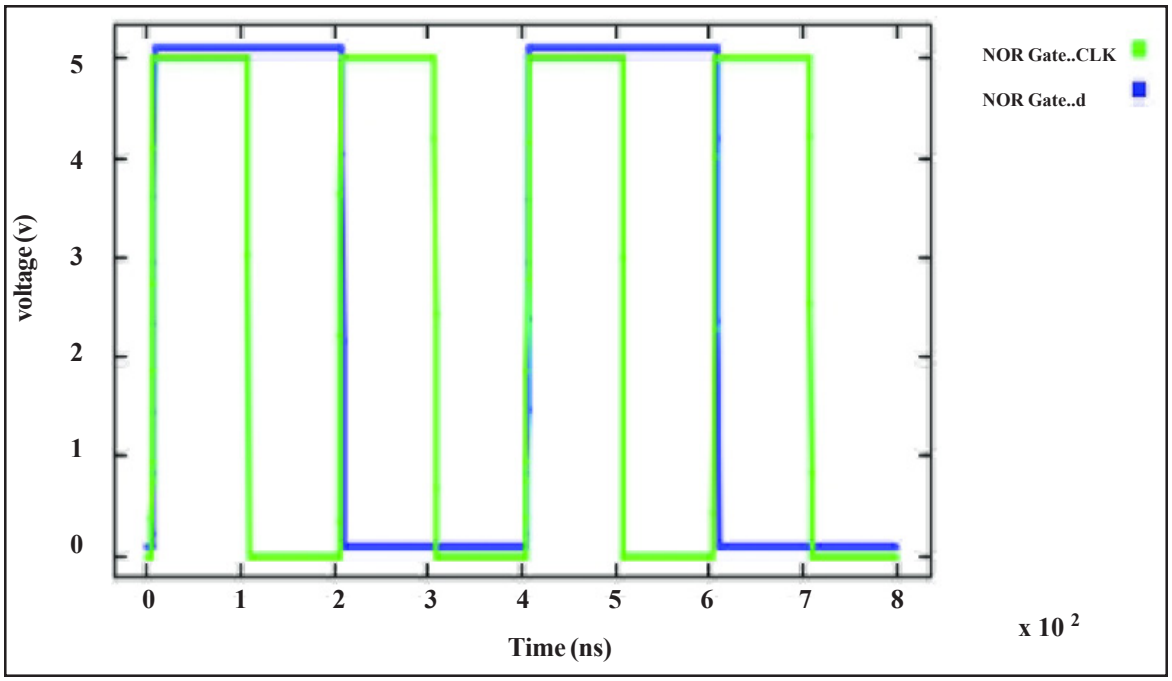
Figure 7. (a) NOR gate (binary sequence 11 and 00); (b) NOR gate (binary sequence 10 and 01)

each basic building block conserving even a few of the transistors will play a major role in area and power improvement of the device. When we talk about area of transistor, it depends upon the following equation.

$$Area = Channel\ Length \times Channel\ Width$$

As we have used HSPICE model of Metal Oxide Semi-conductor Field Effect Transistor (MOSFET). So, the channel length and channel width are already known for 180 nm processing technology. Therefore, we calculated the area of transistor as follows.



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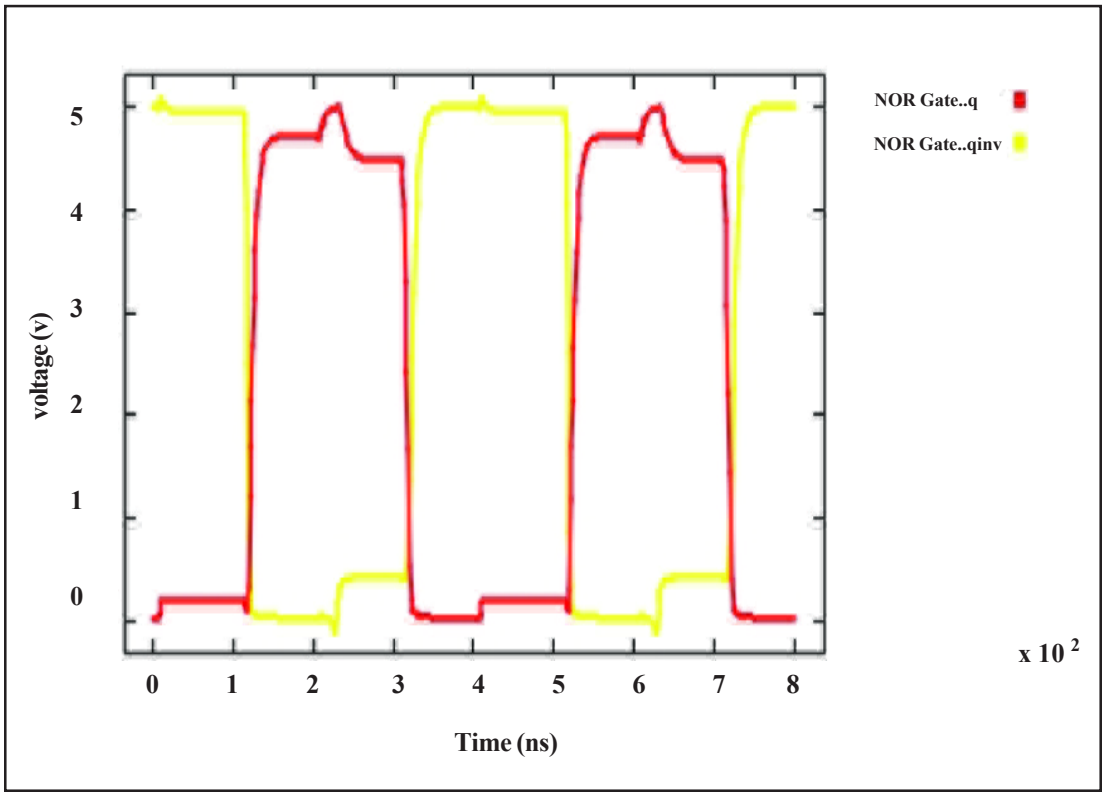

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Figure 8. (a) D flip flop inputs (d and clk); (b) D flip flop outputs (q and qinv)

$$Channel\ Length = 1.8 \times 10^{-07} m$$

$$Channel\ Width = 0.0001 m$$

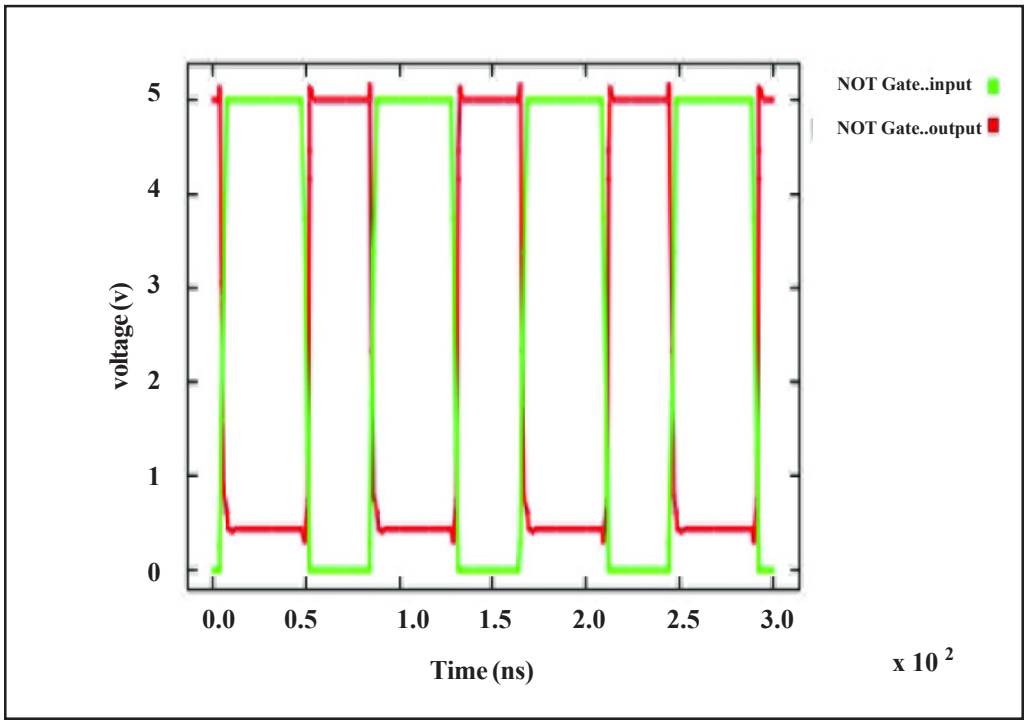
$$Area = 1.8 \times 10^{-07} \times 0.0001$$

$$Area_{Transistor} = 0.018 nm^2$$

Now, based on the discussion presented in [2], [3] and [16], we consider that area of memristor is half of the area of MOSFET.

$$AreaMemristor = 0.009 nm^2$$

Using the schematic diagrams presented in section 3 and discussion presented above, we have calculated areas of hybrid as well as conventional basic building blocks. Table 3 presents a comparison between number of components Transistors) re quired for conventional building blocks and number of components (Memristor+Transistor) required for proposed building blocks. It can be seen from the table that proposed building blocks require less number of components as compared to conventional building blocks. Furthermore, when we incorporate the areas of memristors and transistors from above equations to calculate the areas of these building blocks, results in Table 3 show that proposed building blocks are on average 30% smaller as compared to conventional building blocks. Components mentioned in Table 3, when combined together to form a 2 input tile of FPGA containing CLB, SB and CB, reduces total number of components by 19.2% as shown in Table 4. Conventionally, a 2 input tile of FPGA requires 146 transistors, while the memristor-transistor hybrid approach requires only 59 transistors and 59 memristors. Adding up memristors does use area, but it will be much smaller as compared to transistor. We conserved 28 components in a single tile (2 input). Table also shows the area of a 2 input tile of FPGA, using the above mentioned value of the area of memristor and transistor, we calculate the area of a 2 input tile. According to the Table 4, the area gain of a 2 input single tile is 39%. In Table 4, we have estimated the area gain of a sample single tile only that has a CLB with two inputs and having a



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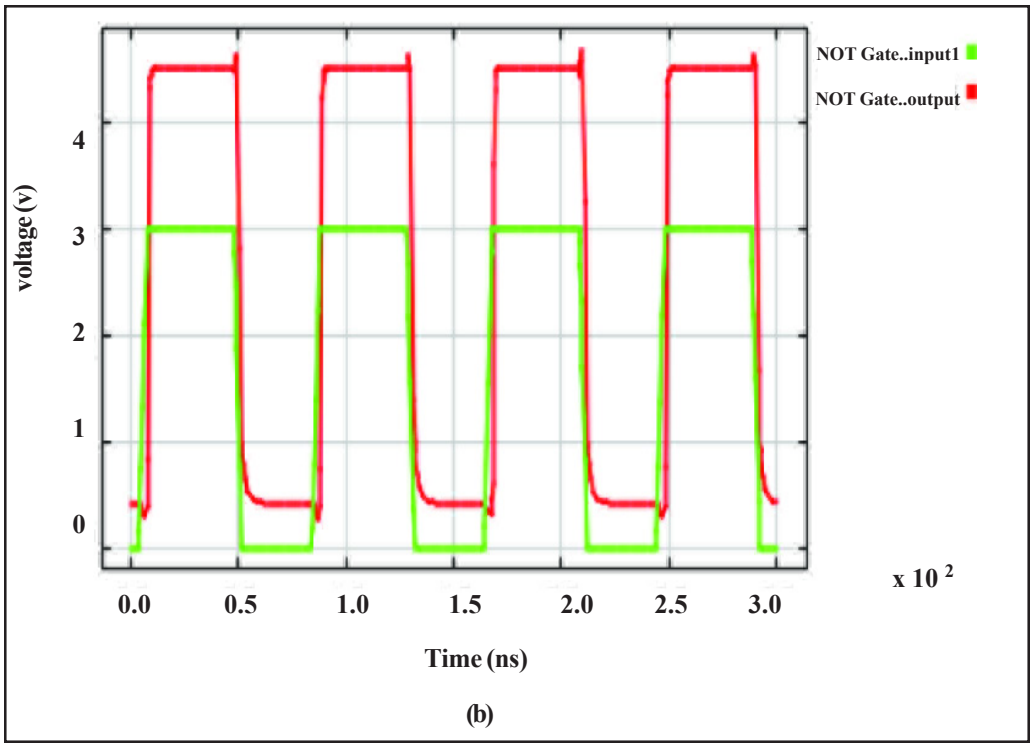

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Figure 9. (a) NOT gate simulation; (b) Buffer simulation

channel width of two only. In real FPGAs, normally there are thousands such tiles each having larger CLB with wider channel widths. So, in that case, our proposed hybrid FPGA will give much better gain as compared to the existing conventional FPGA architectures.

	Power consumption during transition	
Circuit elements	Conventional approach	Proposed hybrid approach
	Watt	Watt
2x1 MUX	8.090E-3	4.104E-3
NOR gate	4.652E-3	1.642E-3
NOT gate	1.873E-3	3.156E-4
Buffer	2.104E-3	4.616E-4
Dflip flop	3.317E-3	1.113E-3

Table 2. Power consumption during transition in conventional and proposed components

	Conventional approach		Proposed hybrid approach		
Circuit elements	No of Transistor	Area nm^2	No of Transistor	No of Memristor	Area nm^2
2x1 MUX	6	0.108	2	2	0.054
NOR gate	4	0.072	2	2	0.054
NOT gate	2	0.036	1	1	0 .027
Buffer	4	0.072	2	2	0.054
D flip flop	30	0.540	15	15	0.405
LUT (2 input)	18	0.324	6	6	0.162

Table 3. Number of components and area comparison in conventional and proposed basic building blocks of FPGA

Circuit elements	Conventional		Proposed		
(Excluding SRAMS)	No of Transistor	Area nm^2	No of Transistor	No of Memristor	Area nm^2
CLB (2 input)	54	0.972	23	23	0.621
Switch Box (2 tracks/channel)	80	1.44	32	32	0.864
Connection Box (2 inputs/side of CLB)	12	0.216	4	4	0.108
Single tile (2 input)	146	2.628	59	59	1.593

Table 4. Number of components and area comparison in conventional and proposed basic building blocks of FPGA for a single tile

4.3 Area Analysis of Memristor-Transistor Hybrid FPGA Architecture

If we know the total number of basic building blocks required for the implementation of particular benchmark on an FPGA architecture, then based on the results presented in section 4.2, we can estimate the area of complete FPGA architecture. For overall area estimation of the proposed architecture, we have customized the design flow presented in [8]. For experimentation, we have used 16 largest MCNC benchmarks. These benchmarks are placed and routed on the proposed FPGA architecture using simulated annealing placement algorithm [22] and pathfinder routing algorithm [23] respectively. After successful placement and routing routing of each benchmark, we have a complete picture of resources required for the implementation of that particular benchmark. Then, we add the areas of individual resources (i.e. areas of basic building blocks) to calculate the overall area of FPGA architecture. Overall area of FPGA is dependent on two areas, routing area and logic area. Furthermore, routing area comprises of buffer area and switching area. We have evaluated buffer area, switching area and logic area of hybrid FPGA for sixteen MCNC benchmarks. Then by adding switching area and buffer area, routing area is calculated. For overall FPGA area, logic area and routing area are added. Table 5 gives detailed logic area, buffer area, switch area, routing area and total area results for memristor-transistor hybrid FPGA architecture. First column gives the names of the sixteen largest benchmarks, next five columns give area results for hybrid FPGA architecture. At the bottom of the table, an average area of memristor-transistor hybrid FPGA is also presented.

Memristor-Transistor hybrid approach					
Benchmark	**Logic Area (nm^2)**	**Buffer Area (nm^2)**	**Switch Area (nm^2)**	**Routing Area (nm^2)**	**Total Area (nm^2)**
Alu	2100	892	12147	13039	15139
Apex2	2592	1100	14971	16071	18663
Apex4	1872	893	12413	13306	15178
Bigkey	1984	461	6601	7062	9046
Des	2592	748	10848	11596	14188
Diffeq	1985	563	8166	8729	10714
Dsip	1984	461	6601	7062	9046
Elliptic	4551	1563	22402	23941	28492
Ex5p	1659	792	11007	11799	13458
Frisk	4901	2069	28189	30258	35159
Misex3	2100	892	12147	13039	15139
Pdc	6635	3086	54786	58592	65227
S298	1873	638	9278	9916	11789
Seq	2464	1172	16295	17467	19931
Spla	5263	2756	39133	41889	47152
Tseng	1557	354	5079	5433	6990
Average	2882	1196	16879	18074	20956

Table 5. Area and Power of memristor-transistor hybrid FPGA (LUT-4) for sixteen MCNC benchmarks

5. Conclusion

In this paper, we have proposed a novel hybrid FPGA architecture. This architecture is based on memristor-transistor hybrid approach. We have designed and implemented memristor-transistor based basic building blocks like 2x1 MUX, NOR gate, D flip

flop, and NOT gate. We have minimized the number of transistors in basic building blocks using memristors which will ultimately reduce the size and improve the power consumption of FPGAs. Ripping the transistor and replacing it with memristor leads to a more efficient FPGA model. For analysis, we have calculated the area and power of memristor-transistor based basic building blocks. Our results show that, on average, proposed building blocks are 30% smaller in area and 60% more efficient in terms of power consumption. We have also calculated the overall area of memristor-transistor hybrid FPGA for sixteen largest MCNC benchmarks using a customized design flow.

In the future, we want to design a complete CAD flow for design and simulation of FPGA architectures that are built using memristor-transistor hybrid approach. We also want to explore and compare memristor-transistor hybrid FPGA with transistor-only FPGA architecture.

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