Design of Low Power Preamplifier Latch Based Comparator

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ABSTRACT: This paper presents a pre-amplifier latch based CMOS comparator design. This design is premeditated to be used as a comparator window. This design is attractive due to its low power dissipation and speed. Preamplifier implies a cascode structure which stabilizes the output voltage and latch with its regenerative feedback which makes comparison fast along with detection of small difference between the inputs. The design is simulated in 90-nm CMOS technology using Cadence EDA software. This design provides a low power of 55 μW with a speed of 55 MHz and supply voltage of 1.2 V.

Keywords: Cascode structure, Low power, Regenerative feedback, Window comparator.

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1. Introduction

Demand for devices with portable battery is increasing rapidly and the crux of matter is low power design methodologies for high speed applications. This power reduction is achieved by voltage scaling. The voltage scaling results in subthreshold region of operation and these increasing demands need to meet in results in new architectures and innovative circuits. As we stepfeatures the performance is affected by process variation. This exists in certain applications like window comparators, analog to digital converters and others. Comparators are the heart of all these applications. Overall performance of comparator is influenced by its design [1]. The important function of the comparator is to compare certain values versus the reference value. Preamplifier based comparators are used for low power design and high speed. The preamplifier stage of comparator improves the sensitivity of comparator from noise generated by feedback stage[2]. The latch stage senses the small difference between the inputs and
detects the larger input. The output buffer provides amplified outputs. An input referred latch offset voltage, resulting from threshold voltage $V_{TH}$, current factor $\beta = \mu C_{OX} W/L$ and parasitic load capacitance mismatches, limits the accuracy of comparators [1]. The design of these stages is very important so as to achieve an efficient performance. In [3], double tail comparator it is proposed where the conventional comparator is changed for low power and quick operation as delay is reduced by adding few more transistors. Common mode input voltage is limited by low power operation.

Comparators with high performance are required to amplify small inputs to signals with sufficient level to be detected by various systems [8]. In the proposed design of the comparator as in [1], a fully differential with an enhanced reset architecture using transmission gates to increase the speed has been used for sample and hold less ADC. A fast comparator with high accuracy is key element for ADC [9]. Apart from technological amendments, designing new circuits for low voltage operation and shunning stacking of transistors between the rails is preferred.

In systems designed for testing and fault detection, window comparators are utilized. They are also required to meet the demand of low power design. The conventional window comparator [4] with voltage hysteresis property operating in noisy conditions employs comparators along with AND gate. Comparators are the vital elements of many electronic systems and it must be optimized to achieve higher performance.

The paper content is organized as follows:

Section 2 describes the different stages of comparator, section 3 represents the simulation result of comparator design along with table of comparison, section 4 discusses window comparator using comparator with some of the results and at last section 5 encloses the paper.

2. Preamplifier Based Comparator Design

The comparator design is major challenge to meet the requirements according to the technology. The preamplifier based comparator circuit has been parted into three stages which are preamplifier stage followed by decision circuit stage that is latch circuit and at last post-amplifier stage.

2.1. Preamplifier Stage

In the design of comparators we consider the first and foremost design of input stage. This input stage is usually known as preamplifier. The main task of comparator is to compare two input signals which may be low or high level signals. When the input signals are fed to the comparator their voltage level should be sufficient enough to be detected and compared with each other, so as to make it comparable we need an input stage that will intensify these signals to make the comparator functional. This increases the sensitivity of comparator. The proposed design of preamplifier has two stages, first one is differential pair and the second stage is cascode stage as shown in fig. 1. The differential pair has two differential inputs $V_{IN1}$ and $V_{IN2}$. The differential pair will increase the bandwidth and at the same time it will reduce the noise. The output of the differential pair is fed to the next stage that is cascode stage. The cascode stage will enhance the gain of the circuit. The reduction in amplification of offset voltage and input noise can be achieved by cascading low gain stage [5].

The drain to source voltage ($V_{DS}$) of the transistors $M_1$ and $M_2$ is fixed as their drain is connected to source of transistors $M_1$ and $M_2$, respectively. The biasing voltage selection is an important factor as it affects output. Gain of the feedback loop is high and can be given as product of transconductance and resistance of transistors involved in feedback loop. The transistors $M_1$, $M_2$ and $M_3$ forms feedback loop which can be seen in fig. 2. The output is thus stabilized. The biasing circuit is used which provides fixed biasing voltages to transistors $M_1$-$M_2$ and $M_7$-$M_{12}$.

When input voltages $V_{IN1}$ and $V_{IN2}$ are applied then corresponding transistors are turned on. The working of circuit in differential mode is as follows. When $V_{IN1}$ is greater than $V_{IN2}$, if the input voltages are enough to turn in the transistors $M_5$ and $M_6$ then both the transistors are on and current through $M_6$ is more than $M_5$ so the output $I_{OUT^-}$ is obtained which is more than $I_{OUT^-}$. When $V_{IN2}$ is greater than $V_{IN1}$ then $I_{OUT^-}$ is greater than $I_{OUT^-}$.

2.2 Latch stage

To accomplish the comparison of two signals the comparator must be able to detect the difference between input signals as small as possible. To attain this capability comparators employ latches. These latches use positive feedback mechanism to accomplish...
comparison and this feedback is commonly known as positive regenerative feedback.

Fig. 2 shows the schematic design of SR latch. While designing the decision circuit, transistor widths were kept minimum that is 120 nm to cater for speed. To retain the circuit in self biased condition, the sizes of transistors were adjusted accordingly. Transistor pair $M_3$, $M_6$, and $M_4$, $M_7$ constitutes the cross-coupled inverter pair structure which act as the main regenerative loop for the latch. For least capacitive effects their sizes of length and width are kept minimum, and W/L ratio is kept as for an ideal inverter. To set the metastable trip point of the inverter to half of the supply voltage sizes are further optimized. Input $IN_1$ is applied on the gate terminals of transistors $M_1$, $M_5$ and $IN_2$ at $M_2$ and $M_8$. Let there be high level voltage at $IN_1$ so transistor $M_5$ will turn driving the output $OUT_1$ to ground. This in turn connected to gate terminal of $M_4$ and $M_7$, gives output $OUT_2$ which is equal and opposite to $OUT_1$. 

![Figure 1. Schematic of preamplifier stage](image1)

![Figure 2. Schematic diagram of SR latch with positive regenerative feedback](image2)
2.3 Output Stage
A fully differential self-biased differential amplifier is used as output stage shown in fig. 3. Differential amplifiers exploit fully differential signals which result in increased noise rejection for noise immunity along with increased gain and output swing. The amplifier inputs are amplified through the inverter amplifiers consisting transistors $M_3$, $M_7$, and $M_6$, $M_{10}$. The biasing of the amplifiers is handled by voltage at the node connecting source of transistor $M_4$ to gate of transistor $M_1$ and $M_2$. This node voltage is due to the device pairs $M_1$, $M_2$ and $M_{11}$, $M_{12}$ which is stabilized by negative feedback loop employing devices $M_4$, $M_5$, $M_6$, $M_{10}$. Utilizing fully differential self-biased amplifiers as output stage gives full swing output without noise and need for reference voltage is banished [11].

2.4 Schematic of the Proposed Comparator
The complete comparator design schematic is shown in fig. 4. Section I is preamplifier stage which amplifies the input signals as input of second stage. Section 2 is latch stage which provides a positive regenerative feedback for high speed and it is responsible for converting input signals to digital level. Section 3 amplifies the outputs of second stage and gives the comparison result.
3. Simulation Results of Comparator Design

In this section simulation results are presented and the circuit is simulated using 90 nm CMOS technology. We have used full scale supply voltage of 1.2 V. $V_{\text{REF}}$ is 0.6 V and input is ramp signal of 0.9 Vpp.

Fig. 5 shows the DC gain of pre-amplifier of 32 dB. Fig. 6 shows the transient response of comparator design where one input is a ramp signal and other input is $V_{\text{REF}}$ of 0.6 V. The comparator design converts the input to square wave of high voltage level of 1.04 V. The output changes its orientation according to input. When the input is lower than the $V_{\text{REF}}$ then output goes to low level logic, when input is greater than reference voltage the output goes to high level logic. The delay is 18.05 nsec with power dissipation of 55 μW.

In digital electronics, for measuring the quality and performance of CMOS circuit power-delay-product (PDP) is a Fig. of merit [6, 7]. It is also termed as switching energy, it is product of consumed power and delay. For calculating PDP we need to calculate power consumption by the circuit and then the time taken by circuit from the instance of giving input and obtaining output. Finally these two parameters are multiplied giving PDP. The PDP of this design is $9.92 \times 10^{-17}$J.
Table 1. summarizes the performances of proposed comparator design at 90-nm technology compared with previous work at different technology.

<table>
<thead>
<tr>
<th>Parameters</th>
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<th>[10]</th>
<th>[7]</th>
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<td>CMOS Technology</td>
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<td>350 nm</td>
<td>180 nm</td>
<td>180 nm</td>
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<td>1.0 V</td>
<td>1.2 V</td>
<td>5 V</td>
<td>1.2 V</td>
<td>1.8 V</td>
</tr>
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<td>-</td>
<td>-</td>
<td>550 ps</td>
<td>-</td>
</tr>
<tr>
<td>Offset Voltage</td>
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<td>-</td>
<td>6.5 mV</td>
<td>7.8 mV</td>
<td>10.24 mV</td>
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</tr>
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</table>

| Table 1. Comparator Performances |

4. Design of Window Comparator

This section describes one of the applications of the comparator. A window comparator circuit consists of one output with two states that is low state and high state, two inputs indicating the high and low limit. When the input is in between the range $V_{\text{LOW}} \leq V_{\text{IN}} \leq V_{\text{HIGH}}$ output is high [4]. The circuit of window comparator has two comparators and one AND gate as shown in fig. 7.

![Figure 7. Window comparator using comparators](image)

There are many applications but most important is used as the input stage of low power SAR ADC with a bypass window for medical applications [4]. In fig. 8 shows the transient response of comparator window. The voltage limits are set to 0.8 V and 0.6 V which indicates higher limit and lower limit respectively.

Ramp signal is fed as input so when the input is in between the limiting voltages that is $0.6 \text{ V} \leq V_{\text{IN}} \leq 0.8 \text{ V}$, we get output of high level equal to 1.20 V.
5. Conclusion

This paper presents a low power pre-amplifier based CMOS comparator architecture simulated in 90-nm CMOS technology using cadence tool. The design is based on preamplifier, latch and output buffer. The cascode design of preamplifier provides a gain of 32 dB with low power consumption of 3.3 μW. The biasing voltage plays vital role in stabilizing the drain voltages which further fixes output voltage of amplifier. The design is simulated with operating voltage 1.2 V. The comparator achieves the dc offset voltage of 0.6 mV with a power dissipation of 55 μW, which is useful in low power applications.

References


