Design of Low Voltage CMOS OTA Using Bulk - Driven Technique

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ABSTRACT: In this paper, we have designed a low voltage CMOS operational transconductance amplifier (OTA) for high speed transmission with an operating voltage 0.5 V. The transistors are operating in the sub-threshold region with source degeneration for transconductance improvement. The OTA achieves a DC gain (Ao) of 26 dB, a gain-bandwidth product (GBW) of 750 MHz, slew rate (SR) of 3.7 V μs, a phase margin (PM) of 98º, DC offset of 2.2 mV and a power dissipation of 250 μW under no load condition. The proposed OTA is simulated in 90-nm CMOS technology using Cadence EDA software.

Keywords: Operational transconductance amplifier; low voltage; sub-threshold; source degeneration.

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1. Introduction

Aggressive scaling of the CMOS circuits, the most widely used remedy to reduce the power dissipation is to decrease the operating voltage to values less than 1 V. Sub-threshold CMOS circuits are best for low power applications as they have good gm/I ratio and have very good efficiency. On the other hand, due to the scaling of the device the supply voltage and the threshold voltage are reduced resulting in degradation of the intrinsic gain. Amplifiers operating at very low supply voltages are best for bio-medical and sensor applications where energy is expected to be harvested from its environment [1]. In bio-medical devices such as ambulatory heart detectors and hearing aids very low power consumption is used to increase the battery life. There is equal importance for low voltage and low power operation in portable applications as low voltage operation enables the use of lesser of batteries thereby being advantageous for size and weight considerations and the battery life gets improved by low power consumption. For low voltage or low power the main idea is to make the circuit operate in the sub-threshold (weak
inversion) region. There are various approaches like floating gate approach, self-cascode structures and bulk-driven transistors. The utilization of bulk-driven differential pair might beat a few requirements forced by supply voltages in situations where its power supply is of the same request as the threshold voltages [2]. Recent publications which are using this technique has provided dependable low voltage and low power amplifiers [1][3]-[7]. Although one of the huge difficulties for the bulk-driven technique is the reduction in $g_{mb}/g_m$ ratio in the CMOS technologies there are some drawbacks of the bulk-driven technique like the value of $g_{mb}$ will be 5-8 times smaller than the value of $g_m$ and very large parasitic capacitance on the bulk and high input referred noise. Therefore, we represent a differential pair operating in sub-threshold region using bulkdriven technique as one possible solution to contend with the $g_{mb}/g_m$ ratio reduction by upgrading the transconductance and enhancing the unity gain frequency ($f_T$) as well as the open loop gain without increasing the power consumption. The principle of the bulk-driven technique is that the input signal is given at the bulk terminal which is less than the threshold voltage and a voltage is being set on the gate terminal so as to form a channel. The thickness of the depletion zone i.e. the conduction channel is affected by the bulk voltage. A bulkdriven symmetrical OTA operating in weak inversion can result in both reduced power consumption and high linearity. For a standard CMOS technology only PMOS can be bulk driven due to the fabrication process. The utilization of the bulk-driven technique makes it conceivable to design lowvoltage OpAmps with very large value of input CMRR and low power dissipation on the CMOS technologies.

In this paper we have used conventional transistors as compared to the halo implanted transistors [1]. Finally, a low voltage OTA using bulk driven technique is simulated with improved various parameters such as slew rate, the effective transconductance, input referred noise, phase margin, as well as improvement in other OpAmp performance parameters.

In section 2, a brief on the basic theory of the bulk driven technique and weak inversion operation is mentioned. In section 3 details of the proposed OTA are described and simulation results are shown and discussed in section 4 of the proposed OTA. In section V, an application approach is simulated using the proposed OTA. Section 6 concludes the paper.

2. Basic Theory Of The Bulk - Driven Technique And Weak Inversion Operation

Bulk-driven MOSFET was first adopted in [8]. While designing an OTA while adopting the bulk-driven technique the most significant stage is the input stage. In this technique, the gate terminal is tied to a fixed bias voltage and the input is given into the bulk terminal as shown in fig. 1. With the zero-bias voltage on the bulk terminal the transistors are in the subthreshold region. The two fundamental favorable circumstances of utilizing the bulk-driven system are that the bulk-driven differential sets in an OpAmp and incredibly enhances the transconductance and the threshold voltage of the transistor vanishes and both negative and positive bias voltages (VBS) are conceivable. For a standard n-well CMOS process, only PMOS devices can be used as a bulk-driven transistor because of the twin tub fabrication process. Whereas there are a couple of downsides to the bulk-driven technique when contrasted with the gate driven method, for example, little transconductance due to the less input capacitance of the depletion layer and larger parasitic capacitance to the mass which diminishes the $f_T$. Due to the smaller transcondacnace the device will have high input referred noise. By setting the input signals on the substrate instead of gate terminals the input differential pair will results in large input CMRR of the OpAmp. The enhancement in the transconductance is determined by the positive feedback.

The drain current $I_{DS}$ of the MOS transistor operating in weak inversion is based on a channel diffusion current that can be expressed [2] as

$$I_{DS} \exp \left( \frac{qV_{GS}}{nkT} \right) \exp \left[ \frac{q(n-1) V_{BS}}{nkT} \right]$$

(1)

Where $n$ is the slope factor in sub-threshold, which can be defined as $1+g_{mb}/g_m$ it is in fact not a consistent variable but rather a component of the process parameters and substrate biasing [9]. The effect of $V_{BS}$ on the current $I_{DS}$ is lower by the component (n-1) contrasted with the $V_{GS}$. This gives fundamental further point in expected transconductance in the bulk-driven circuits. The transistor will be operating in weak inversion when $V_{BS} > 3kT/q$ [9]. This paper presents simulated results only of an improvement in the transconductance for input bulk-driven differential pair. The transconductance of the differential pair is defined as

$$G_m = \frac{dI_o}{dV_{in}}$$

(2)
Figure 1. Bulk-driven nMOS

Where \( I_o \) is the output current and \( V_{in} \) is the input voltage. As the CMOS scaling is done, the ratio of \( g_m \) and \( g_{mb} \) decreases, however the improvement element \( \frac{n+1}{(n-1)} \) ratio increments demonstrating the overall transconductance will increment with scaling.

3. Proposed - Bulk Driven Ota Circuit

Figure 2. Circuit diagram of the proposed operational amplifier
Fig. 2 shows the circuit diagram of the proposed bulk-driven OTA circuit. The proposed OTA consists of two differential pairs. The input signal is given on the bulk terminal of the p-type transistors in the first differential pair. It consists of four p-type transistors. The four transistors are represented as $M_{1a}$, $M_{1b}$, $M_{2a}$, $M_{2b}$. The transistors $M_{1a}$ and $M_{2a}$ are identical, whereas the $M_{1b}$ and $M_{2b}$ are also identical. The drains of the $M_{1b}$ and $M_{2b}$ are connected to the other differential pair. The reference current ($I_{\text{REF}}$) is given as 500 $\mu$A. Moreover, the slew rate to the amplifier is determined by the reference current. The main objective of the proposed OTA is that all the transistors should work in sub-threshold region or the weak inversion region. The circuit has a operating voltage of 0.4 V. The PMOS transistors are used as active load of differential pair is given by two identical transistors $M_3$ and $M_4$, they are split into four transistors, the active loads $M_{3a}$ and $M_{4a}$ and the common gate (CG) amplifiers $M_{3b}$ and $M_{4b}$.

There is an expansion in the DC shift for higher swing and high output impedance. The last stage comprises of transistor $M_6$ as the input transistor and transistor $M_7$ as its active load. The compensation circuit consists of a capacitor of 100fF. The capacitor $C_c$ is placed inside the output stage to establish the dominant pole associated. The location of the dominant pole is pushed to a lesser value due to Miller effect of the capacitor $C_c$. It is basically an on-chip amplifier. The Bandwidth of the proposed OTA is significantly very large, which therefore leads to higher gain bandwidth product (GBW). The frequency should be high for the design of OTA such that the total phase margin of more than 60 f can be obtained.

4. Simulation Results

Fig. 3 represents the transient response of the proposed OTA with the operating frequency of 100 Hz, 10-mVpp input to only the inverting input terminal. The rise time is about 10 ns. Fig. 4 shows the simulated bode diagrams for the proposed bulk-driven OTA. The output impedance do not depend on the bulk-driven differential pair and change in open loop gain. The unity gain frequency is dependent to the change in transconductance. The gain of the proposed bulk driven OTA is less which is a disadvantage of the circuit. But there are other parameters which are having good value. The reference current is 500 $\mu$A with the power supply of 0.4 V, allowing all the transistors operating in weak inversion. All nMOS and pMOS threshold voltages are 80 mV and 140 mV respectively.

![Figure 3. Transient response of the OTA](image-url)
Figure 4. Simulated bode diagrams for the proposed bulk-driven OTA

Figure 5. Variation of the output current with change in the temperature
Fig. 5 demonstrates the change on the output current with change in the temperature. The simulated results verify that there is an increase in the output current as the temperature is increasing. At $T=0^\circ F$ the output current increases and becomes constant when the input voltage is 0.5 V. At $T=20^\circ F$ the output current increases and decreases when voltage is 0.5 V. Current variation is shown with change in temperature. The PSRR performance is also simulated when the conditions are $V_{DD} = 0.5$ V and no load condition. The simulated result is shown in Fig. 6. The proposed OTA with bulk driven technique achieves a PSRR of 54.5 dB at low frequencies whereas the roll-off frequency is $\sim 100$ Hz.

Table 1. lists the performance comparisons between the proposed OTA and several previous papers. The analysis is done by using Cadence tool. The PSRR of the proposed OTA is -54.5 dB at 100 Hz. The value of PSRR reduces at high frequencies. The circuit is having high PSRR due to the output capacitance. The value of the PSRR is directly proportional to the output capacitance. Due to the value of biasing current, high slew rate of the proposed bulk-driven OTA is achieved. The equation (3) shows the pole frequency expression $f_{\text{roll-off}}$ of the bulk-driven proposed OTA can be given by

$$f_{\text{roll-off}} = \frac{g_m b}{2\pi C_L}$$

5. V-I Convertor By Using Bulk - Driven Ota Circuit

Fig. 7 shows the most simple configuration of a V-I converter. The design is made out of a buffered voltage divider before the V-I converter. Attenuation of the input voltage is done by a rail to rail input voltage divider before the V-I converter. The V-I converter is thereby essentially composed of two V-I converters in cascade. The functioning involves the input voltage $V_{in}$ being buffered to the OTA voltage follower with the input-output voltage being rail to rail. A modular circuit can be set only with cascode configuration so that in the second phase the cascode transistors can enhance the current being copied and increase output resistance. The voltage divider formed of resistors attenuates the voltage being buffered given by the formula.

$$\alpha = \frac{R_2}{R_1 + R_2}$$
### Table 1. Proposed Ota Performance Comparison

<table>
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<td>440 μS</td>
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<td>&lt; 10 nA</td>
<td>&lt; 3 nA</td>
<td>2.15 nA</td>
<td>&lt; 10 nA</td>
<td>&lt; 1 nA</td>
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<td>DC gain</td>
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<td>Phase margin</td>
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<td>98°</td>
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<td>Slew rate</td>
<td>2.53 V/μs</td>
<td>0.64 V/μs</td>
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<td>DC offset voltage</td>
<td>8.4 mV</td>
<td>2.8 mV</td>
<td>1.3 mV</td>
<td>10 mV</td>
<td>2.2 mV</td>
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<tr>
<td>Input referred thermal noise</td>
<td>0.2 mV/√Hz</td>
<td>3.3 mV/√Hz</td>
<td>0.9 mV/√Hz</td>
<td>165 nV/√Hz</td>
<td>180 nV/√Hz</td>
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<td>PSRR</td>
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<td>54.5 dB</td>
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<td>GBW</td>
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<td>n.a</td>
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<td>Power consumption</td>
<td>197 μW</td>
<td>18 nW</td>
<td>358 μW</td>
<td>130 μW</td>
<td>250 μW</td>
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</table>

Table 2. V-I Convertors Performances

The voltage is buffered to

\[ V_A = V_{in} = \alpha V_{in} = \alpha V_{in} \]

Then, the generated current \( I_1 = \alpha V_{in} / R_s \).

The FoM from [13] can be expressed as

\[ \text{FoM} = \frac{V_{in}}{VDD} \times \frac{BW}{\text{power}} \]

Publications published recently which are linear rail-to-rail V-I converters derived by implementing passive resistors at the input terminals [10][11].
6. Conclusion

In this paper a low voltage OTA using bulk-driven input differential pair is presented. The circuit is simulated in 90-nm standard CMOS process using Cadence EDA software. The methodology utilized a source degeneration of a positive feedback in a differential pair to enhance the transconductance and the slew rate. The change in the transconductance, the execution parameters of the OpAmp, for example, slew rate, UGBW, GBW are all upgraded. The GBW of the OpAmp is 750 MHz and the slew rate is 3.7 V/μsec while achieving a PSR of ∼55 dB with a 0–100-kHz frequency range. The power consumption is 250 μW with a supply voltage of 0.5 V making this OpAmp very useful in high speed transmission and biomedical applications.

References


