Editorial

We are pleased to release the third issue of the **Journal of Electronic Systems**.

In the first paper on **"Design of Low Power Preamplifier Latch Based Comparator"** the authors *Siddharth Bhatt, Shubam Choudhary* and *Jayakumar Selvakumar* have designed a pre-amplifier latch based CMOS comparator. They have simulated the design in 90-nm CMOS technology using Cadence EDA software and recorded low power and high speed.

In the second paper on "**Design of Low Voltage CMOS OTA Using Bulk - Driven Technique**" the same authors have designed a low voltage CMOS operational transconductance amplifier (OTA) for high speed transmission with an optimum operating voltage. The proposed OTA is simulated in 90-nm CMOS technology using Cadence EDA software and found good results.

Adeel Saleem and his colleagues in the last paper on "**Wide area Protection and Monitoring in Smart - power – grid"** proposed the Wide area Protection in smart-power-grid. Some of the key technologies like wide area measurement system and wide area communication system are analyzed in the paper.

The papers of this issue are marked by the technical increments.

Editors