Output Variation Compensation of Bandgap Voltage Reference for Efficient Calibration Strategy

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ABSTRACT: *The voltage reference represents a very important stage in applications such RF system. Most bandgap voltage reference designer use bipolar junction transistors (BJT) to easily reduce the temperature dependence and supply voltage, other use an operational amplifiers (OP-AMP), which are generally very complex and may present undesirable parasite and high power consumption. This paper presents a approach for output variation compensation of bandgap voltage reference. The proposed technique is considered as an efficient calibration strategy for the BGR used to minimize the chip size and current consumption.*

Keywords: Bandgap voltage reference, Compensation, Temperature, Supply voltage

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1. Introduction

A voltage reference is an important block in many digital, analog and mixed-signal circuits. The demand for stable voltage reference is especially apparent in RF analog building blocks such as phase-locked loops (PLLs), oscillators, amplifiers. Hence, the voltage reference circuit must be constant and accurate. However, it is insensitive to the variation of the supply voltage and the temperature production process, etc…

The most used bandgap voltage reference circuits use BJT or parasitic BJT in CMOS process [5] [3], as well as op-amp [3] [8][10] and also lateral bipolar transistors [6]. This has resulted in the development of new output voltage reference-compensated techniques, such as exponential temperature compensation [11],quadratic temperature compensation [10], curvature compensation techniques are used in [14, 15, 16], piecewise-linear curvature correction [12], [13], which are generally very complex and may present undesirable parasite and high power consumption. With the reduction of the transistors size, this paper presents a new approach for output variation compensation of bandgap voltage reference.

The rest of the paper is organized as follows. Section 2 describes CMOS voltage reference circuit design. Section 3 discusses the variation of the voltage reference. The compensation of the output of bandgap voltage reference is described in Section 4. Simulation results and discussion are demonstrated in section demonstrated in section 5. Finally, a conclusion is provided in section 6.

2. CMOS Voltage Reference The Bandgap Voltage Reference Circuit Is Shown In Figure 1 [1].

Both Transistors M6 **,** M5 and M4 are connected as current mirrors and served for realizing the function of self biasing, they enforce branch currents equal to a PTAT I. In order to stabilize the circuit behavior with corner and Vdd variation, transistors

M7 and M8 force “1” node voltage to be equal to “2” node voltage. Resistors R1 and R2 implement the temperature compensation. Transistors M1 and M2 which operate with M3 in weak inversion produce the circuit current and make possible to transistor M3 to be stable and preserve the voltage with Vdd variation. The output voltage is given by:

$$V_{ref} = V_{DS_{M8}} + R_2 I_{PTAT} \quad (1)$$

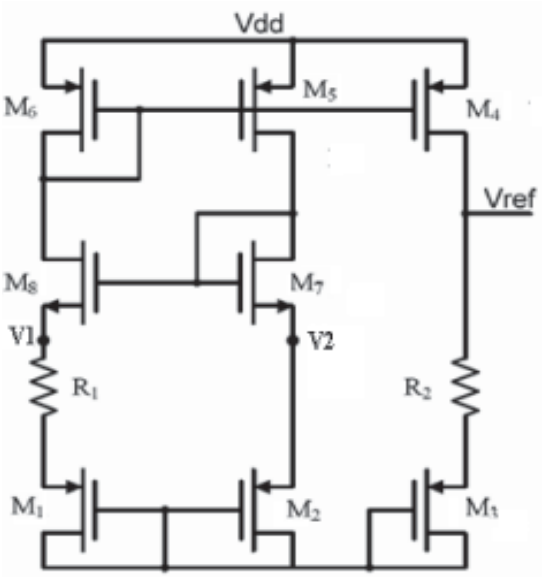

Figure 1. Simple implemented of bandgab reference

3. Variation Of Voltage Reference

The reference voltages are blocks of analog and mixed service that are used in various applications. These circuits must be stable despite variations in temperature and feeding. Indeed, the specifications of the various active devices (gain, transition, frequency, etc ...), set by currents or reference voltages, must meet the specifications, first for a range of temperatures typically ranging from 0°C to 70 °C for a circuit-based consumer and -55°C to 125°C for a circuit for military purposes, and secondly to supply voltages generally within ± 10%.

3.1 Output voltage versus temperature

The drain-source current Ids of a PMOS transistor in weak inversion and saturated (Vds>>KT/q) is based on the channel diffusion current and can be given by the following expression:

$$\begin{aligned} Ids(T) &= \mu C_{ox} V_T^2 \frac{W}{L} \exp\left(\frac{Vgs(T) - Vth(T)}{\eta V_T}\right) \\ &= I_0 \frac{W}{L} \exp\left(\frac{Vgs(T) - Vth(T)}{\eta V_T}\right) \end{aligned} \quad (2)$$

Where I0 is the characteristic current, η is the slope factor in weak inversion, V_T (V_T =KT/q) is the thermal voltage, and symbols W, L, Vgs and Vth, have their usual meaning. From the above equation the expression of the gate–source voltage Vgs is given by:

$$Vgs(T) = Vth(T) + \eta V_T \ln\left(\frac{L}{W}\frac{Ids(T)}{I_0(T)}\right) \quad (3)$$

From the circuit it is possible to extract the PTAT current equations:

$$I_{PTAT}=\frac{Vgs_6(T)-Vgs_7(T)}{R_1(T)} = \frac{\eta V_T}{R_1(T)}\ln\frac{k_7}{k_6} \quad (4)$$

Where

$$k_i=\frac{w_i}{L_i} \quad (5)$$

A diffusion or a poly resistor presents a linear dependence on the temperature [7], as illustrated in the following equation, where φ is the temperature coefficient that depends on the CMOS process [4]:

$$R(T)=R(T_0)[1+\varphi(T-T_0)] \quad (6)$$

Where T_0 is the room temperature and it is considered as 300K.

From the above mentioned the characteristic current I_0 is proportional to the square of voltage V_T and the electrical mobility μ, which in turn is dependent on the temperature.

$$I_0(T)\propto\mu(T)\left(\frac{KT}{q}\right)^2 \quad (7)$$

Therefore, the current I0, as a function of the temperature, can be illustrated by the following equation [4]:

$$I_0(T)=I_0(T_0)\left(\frac{T}{T_0}\right)^{\alpha} \quad (8)$$

Where α is a process-dependent parameter that relates the characteristic current to the temperature [7] [9] [4]. Based on expression (8), the drain-source current is given by:

$$Ids(T)=Ids(T_0)\left(\frac{T}{T_0}\right)^{\alpha}\exp\left(q\frac{Vgs(T)-Vth(T)}{\eta KT}-q\frac{Vgs(T_0)-Vth(T_0)}{\eta KT_0}\right) \quad (9)$$

The threshold voltage can be referred to a room temperature T_0 through a first-order approximation [4]:

$$Vth(T)=Vth(T_0)-\theta(T-T_0) \quad (10)$$

Where the coefficient , depends mainly on the substrate doping and it is valid for the 200–400K temperature range [7] [9] [2]:

Equation (9) can be rewritten with the aid of expression (10) in order to derive an equation for gate–source voltage V_{gs} as a function of the temperature, as given by:

$$Vgs(T)=(Vth(T)+\theta T_0)\left(1-\frac{T}{T_0}\right)+Vgs(T_0)\left(\frac{T}{T_0}\right)+\eta\frac{KT}{q}\ln\left[\left(\frac{T}{T_0}\right)^{\alpha}\frac{Id(T)}{IdT_0}\right] \quad (11)$$

Substituting (4) and (11) in (1), the expression of the reference voltage Vref can be written as follows:

$$V_{ref}=(R2(T_0)+\varphi(T-T_0))\frac{\eta V_T}{R_1(T)}\ln\frac{k_7}{k_6}+(Vth(T)+\theta T_0)\left(1-\frac{T}{T_0}\right)+Vgs(T_0)\left(\frac{T}{T_0}\right)+\eta\frac{KT}{q}\ln\left[\left(\frac{T}{T_0}\right)^{\alpha}\frac{Id(T)}{IdT_0}\right] \quad (12)$$

Since the Vgs voltage of a PMOS transistor in weak inversion has an almost linear behaviour that decreases with the temperature, V_T increases linearly with temperature, a low temperaturedependence Vref can be obtained by scaling up V_T and adding it with Vgs as shown in figure 2.

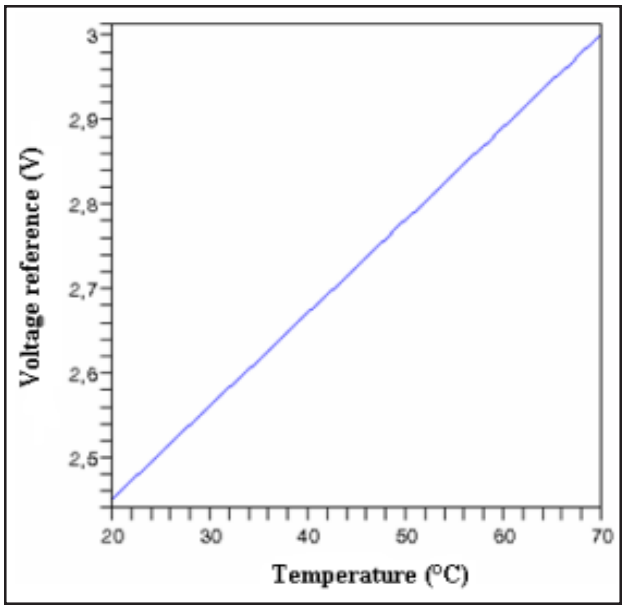

Figure 2. Temperature dependence of the bandgap reference

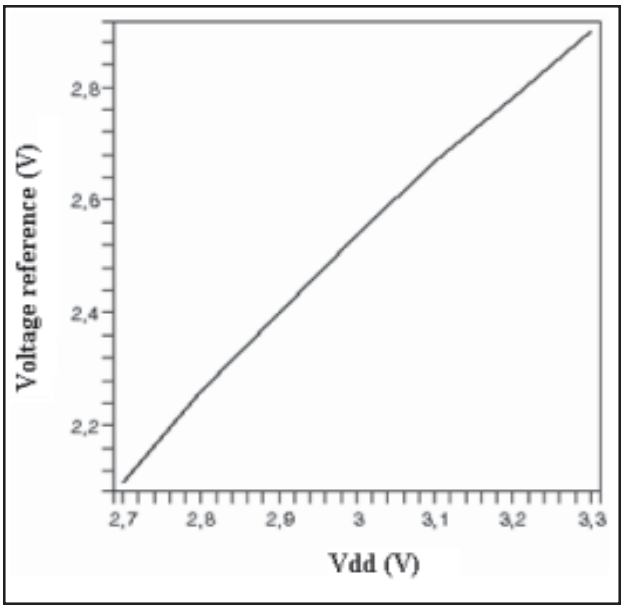

Figure 3. Voltage reference against supply voltage

This figure shows the simulated reference voltage as a function of temperature in the range from 20 to 70°C (Vdd=3V). The Vref increases with temperature. This deviation is about 0.5V.

3.2 Output voltage versus Vdd

The voltage supply variation is ±10%. The variation of Vdd will affect Vds and Vgs of the MOS transistors, which in turn also change the current I_{PTAT} and finally the voltage reference Vref. Figure 3 shows the influence of the supply voltage variation to reference voltage.

This figure shows that the voltage Vref varies with Vdd. In fact, such a decrease (or increase) by 10% at the desired value of supply voltage, it results a decrease by 0.4 V at the voltage Vref (or increase by 0.4V).

4. Variation Compensation Of Voltage Reference

To the needs to provide a voltage stable and precise independent of temperature and supply voltage, we calibrate the reference voltage by varying the resistor R2.

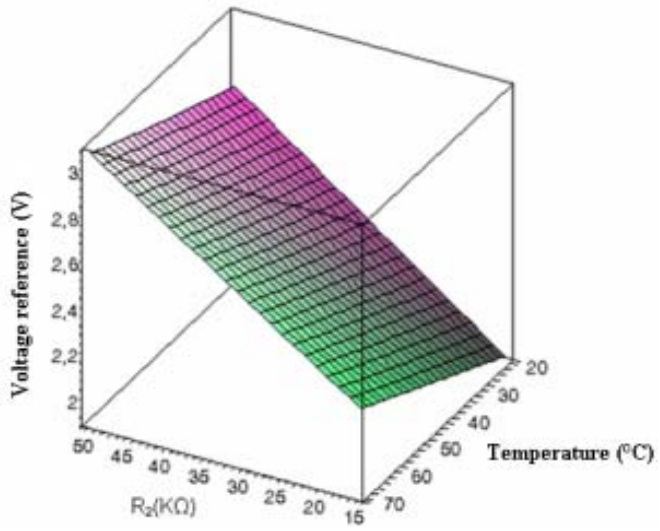

Figure 4. Voltage reference variation vs R2 and temperature

Figure 4 presents the reference voltage vs the resistor R2 and temperature. It is clearly seen that the reference voltage increases with R2 and temperature. Then it is enough to vary this resistance to calibrate Vref.

From the above mentioned, we notice that, the resistors value varies from corner to corner. The trimming is done with the correct resistor calibration as shown in figure 5**.**

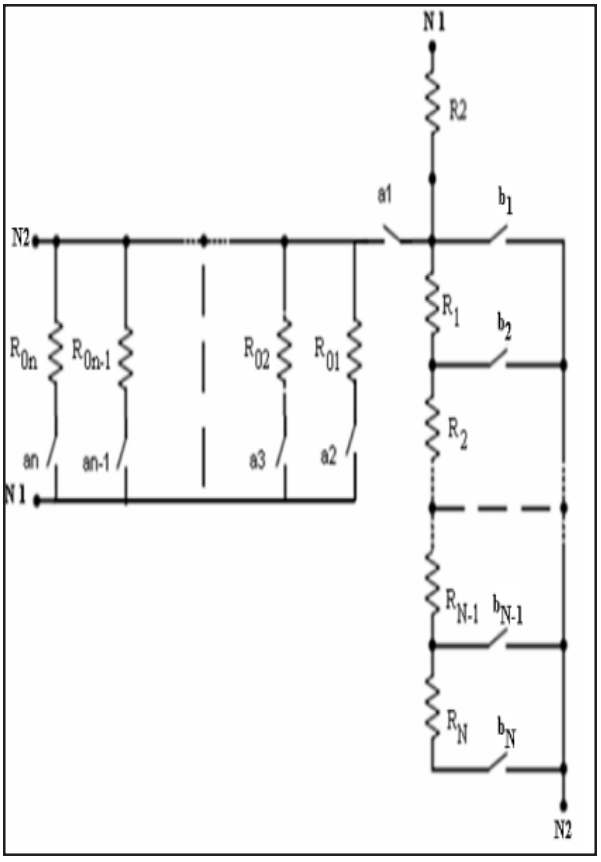

Figure 5. Technique adapted for varying the resistor R2

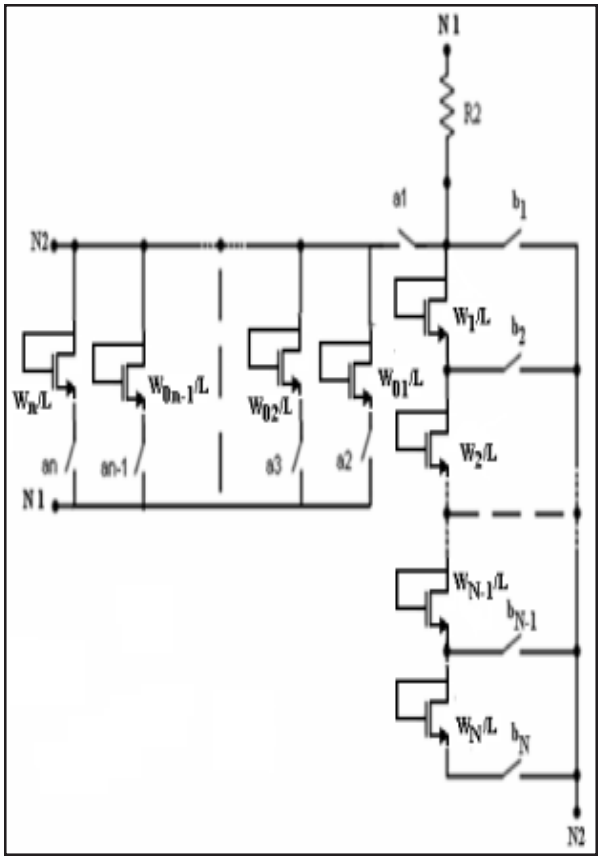

Figure 6. Technique adapted for varying the resistor R2 using diode connected NMOS transistor

However, this method suffers from difficulty in integrating the resistor especially if it has great value in the range of 20kΩ. Indeed, the integration of resistance requires a large space on chip.

While continual scaling of transistor dimensions has improved, we replace the resistor by a diode connected NMOS transistor (figure 6) as illustrated in the following equation:

$$R2 = \frac{1}{gm} = \frac{1}{\sqrt{2\mu_n cox \frac{W}{L} I_d}} \qquad (13)$$

Figure 7 presents the resistor R2 (1/gm) vs Id and W. It is clearly seen that when R2 increases, W and Id decrease.

Thus, our proposed technique is considered as an efficient compensation strategy for the bandgap voltage reference used to minimize the chip size and current consumption.

5. Simulation Result And Discussion

Figure 8 shows the resistor of calibration as function of temperature. The curve connecting these two parameters is monotonic, hence we can determine the relationship between the temperature and the value of calibration resistor desired ($Rc = R2 + R_{i,\ i = 1\ ..\ N}$ or $Rc = R2\ //\ R_{0j,j = 1\ ..\ n}$ according the voltage reference compensation).

The expression of the calibration resistor Rc (KΩ) as a function of temperature is given by:

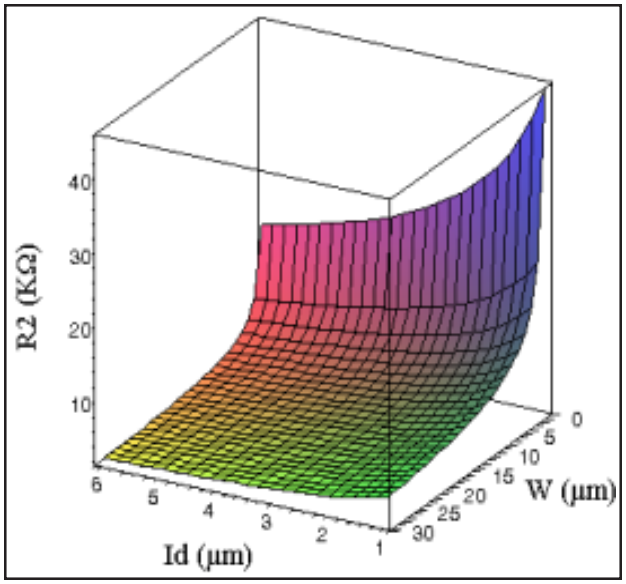

Figure 7. Value of R2 (1/gm) vs Id and W

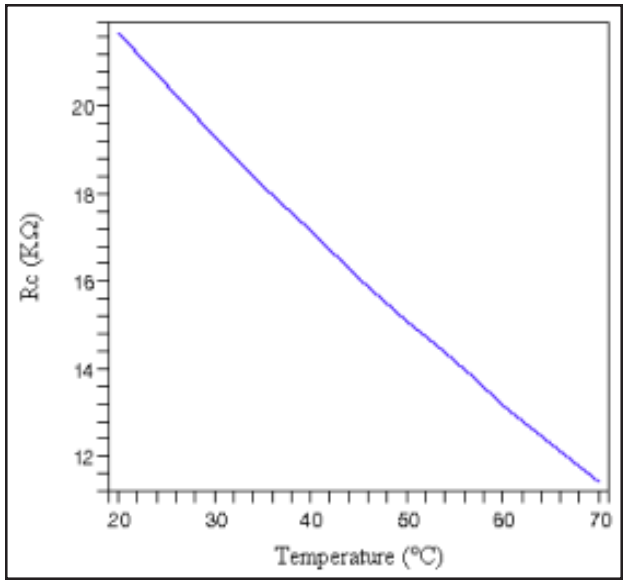

Figure 8. Calibration resistor Rc vs temperature

$$RC = -0.24\,T + 26.15 \quad (14)$$

6. Conclusion

We have presented a calibration technique on CMOS bandgap voltage reference which allows the compensation of BGR output variation.

The proposed technique is considered as an efficient calibration strategy for the BGR used to minimize the chip size and current consumption.

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