A High Gain and Low Noise UWB LNA for 3.1-10.6 GHz Wireless Application in 130 nm CMOS Technology

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ABSTRACT: *In this paper, a high gain and low noise 3.1-10.6 GHz ultra wideband (UWB) CMOS low noise amplifier (LNA) with common gate (CG) topology was designed, which adopted a T-match input network of 50© matching in the required band. The power reduction is achieved by the current reused technique. The proposed LNA was fabricated using TSMC 130 nm CMOS technology. The simulation results demonstrated a power gain of 21.603 dB with a ripple of ± 1.02 dB, achieved noise figure less than 3.168 dB, an input return loss less than -15.576 dB and output return loss less than -20 dB. With a power supply of 1.2V, the proposed circuit consumes 5.82 mW.*

Keywords: Low noise amplifier, UWB, Common gate, Current reuse, CMOS

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1. Introduction

Since the Federal Communication Commission (FCC) has allocated 7.5 GHz bandwidth for UWB application in the unlicensed frequency range of 3.1-10.6 GHz, the related technologies have attracted much attention from both industry and academia [1]. This technology has become more popular for broadband wireless communication research due to the main characteristics of UWB systems include low power spectral density, short duration pulses, robustness to multipath fading, and particularly the high data-rate short-range communications.

The increasing demands on portable wireless devices have motivated the development of CMOS Radio Frequency Integrated Circuits (RFICs), these portable devices require low power dissipation to maximize Buttery lifetime [2]. LNA is the first stage of any communication receiver, so the LNA plays a vital role because the quality of the signal that is received and pre-amplified is a critical factor in the overall system performance [3]. The LNA can be directly added to the first stage in the receive path, it usually dominates the NF and bandwidth in the receiver, and it often makes a trade-off among gain, noise and bandwidth [4]. The UWB LNA has several requirements, such as sufficient wideband input return loss, output return loss, sufficient flat gain over the entire 7.5GHz bandwidth, low noise figure for sensitivity, low power consumption for mobility, and a small chip area for low cost. Many topologies have been presented in LNA designs, such as distributed amplifiers [5, 6], resistive shunt feedback [7], cascade amplifiers [8], and current reused amplifiers [1,9]. The distributed amplifier can improve gains at higher frequencies and hence can extend the bandwidth. But it needs more inductors and thus consumes for broadband amplification including gain flatness, stability, noise figure, and matching. The resistive shunt feedback amplifier can achieve good input matching, high gain and wideband performance. Unfortunately, the performance is degraded when the amplifier is operated in the high frequency band,

this is due to the effect of parasitic capacitances [10, 11].

In this paper, we present a UWB LNA fabricated in TSMC 130 nm CMOS technology. The proposed UWB LNA adopts the CG topology and utilizes current reused technique to achieve low power consumption, a peak gain of 22.622 dB and a minimum NF of 2.879 dB in 3.1-10.6 GHz. The T-match and current reused technique are adopted to achieve inter-stage matching, and to further reduce power consumption.

2. Circuit Design and Analysis

2.1 Noise Analysis

We can characterize the performance of a particular receiver element by its NF, which is the ratio of actual output noise of the element to that which would remain if the element itself did not introduce noise. The total NF of a receiver system (a chain of stages) can be calculated using the Friss formula as follows:

$$NF = NF_1 + \frac{(NF_2 - 1)}{G_1} + \frac{(NF_3 - 1)}{G_1 G_2} + \ldots + \frac{(NF_n - 1)}{G_1 \cdots G_{n-1}} \qquad (1)$$

The total system NF equals the sum of the NF of the first stage (NF1) plus that of the second stage (NF2) minus 1 divided by the total gain of the previous stage (G1) and so on. This result suggests that the noise contributed by each stage decreases as the total gain preceding that stage increases, implying that the first few stages in a cascade are the most critical. It is understandable that the total NF is dominated by the NF1, which is the NF of the LNA

2.2 Input Impedance Matching network

The input stage of the UWB LNA is critical to achieve low noise performance with almost flat forward power and input matching over the entire UWB frequency range. The well-known common source (CS) and the CG topologies are rigorously employed by designers as an UWB LNA input stage [12,13,14].

Recently, CG LNAs have become more and more popular for UWB systems thanks to their simpler input matching network (IMN), better linearity, lower power consumption, and better input output isolation compared with CS LNAs. However, it suffers from channel noise and poor gain response because of the restricted value of the transconductance available for input matching.

Obtaining wideband matching is crucial to an UWB system. Conventional CG LNA primarily uses the inductance L_s for extending the input matching band by resonating with the gate-source parasitic capacitance C_{gs} of transistor M_1 at the band of interest. In Fig. 1 (a), the input impedance of the conventional CG topology is estimated as:

$$Z_{\text{in}} = j\omega L_S \,//\, \frac{1}{j\omega C_{gs}} \,//\, \frac{r_0 + Z_L}{1 + g_{m1} r_0} \qquad (2)$$

Where g_{m1} is the transconductance of $M1$ and $r0$ is the channel resistance of $M1$. Under the matching conditions, if the channel length modulation and body effect are neglected, then the input impedance is estimated as:

$$Z_{in} = \frac{r_0 + Z_L}{1 + g_{m1} r_0} \approx \frac{1}{g_{m1}} \qquad (3)$$

For the normal CG amplifier, the ideal value of gm1 is 20 mS in order to achieve 50W input matching. However, impedance matching is a challenging task in a wideband application; in particular, when the gm1 value is different from 20 mS, the input impedance cannot match the source impedance. On the other hand, in deep-submicron CMOS technologies, $g_{m1} r_0$ rarely exceeds 10 and that allows $R_L / g_{m1} r_0$ to become comparable with or even exceed $1/g_{m1}$. Furthermore, the voltage gain of CG LNA is proportional to g_m, and the noise factor is inversely proportional to g_m [15]. Therefore, we try to alleviate the restricted g_m value by a simple IMN topology as shown in Figure1 (b). Its equivalent small signal model is shown in Figure 2. In Figure 1 (b), we propose a CG LNA architecture, which adopted a new T-match IMN composed of a series L_S- R_S, interconnection-line inductance L_1, and C_{gs}- g_{m1} of transistor M_{11} to enhance the matching bandwidth of the IMN LNA. In addition, the self-body bias technique is used to reduce power consumption further.

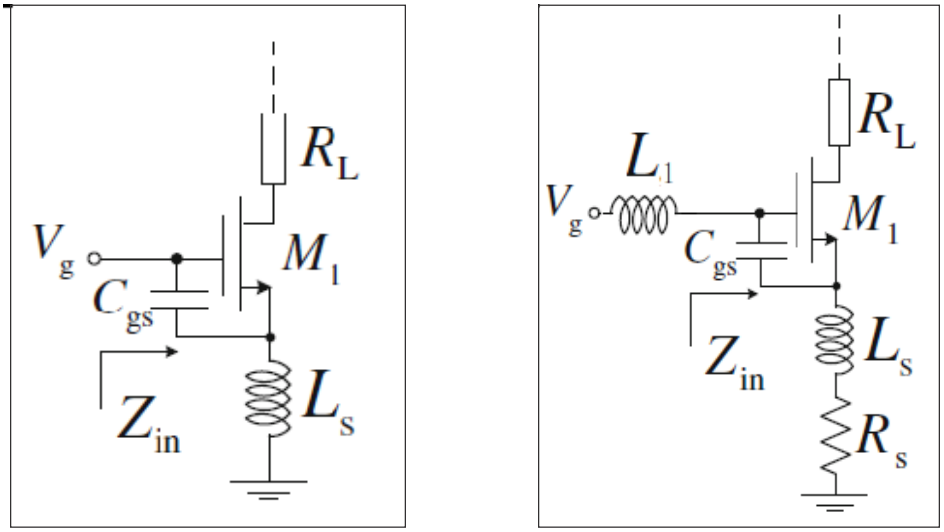
The input impedance looking into the circuit from the source of transistor M_1 is derived as follows:

$$Z_{\text{in}} = jwL_1 + [(j\omega L_S // R_P) // \frac{1}{j\omega C_{gs}}] // \frac{r_0 + Z_L}{1 + g_{m1} r_0} \quad (4)$$

Where, $R_P = \frac{L_S^2 \omega^2}{R_S} + R_S$.

While C_{gs1} resonates with L_S, the input impedance can then be approximated as:

$$Z_{\text{in}} = jwL_1 + R_P // \frac{1}{j\omega C_{gs}} // \frac{r_0 + Z_L}{1 + g_{m1} r_0} \quad (5)$$



(a) conventional CG LNA (b) the proposed IMN topology

Figure 1. CG LNA Topology

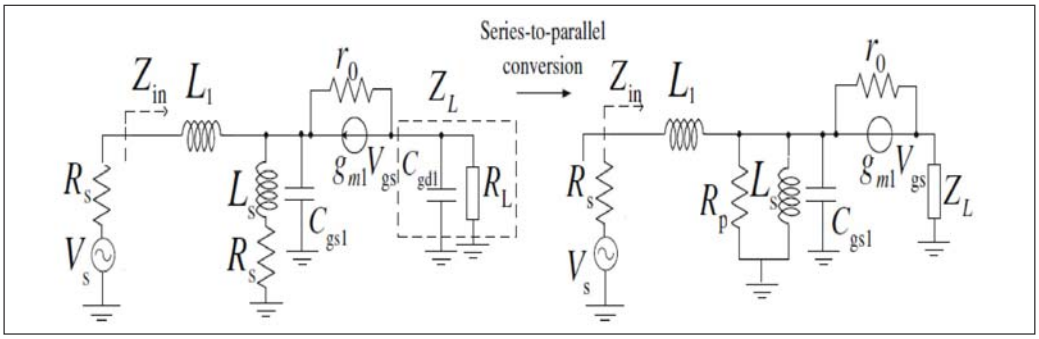


Figure 2. The equivalent small signal model of the circuit in Figure 1(b)

It can be observed that R_p adds an additional degree of freedom to the input match design, and alleviates the restricted g_{m1} value for input matching. Equation (5) illustrate that g_{m1} is not restricted to 20 mS if resistance *R*s is adjusted to maintain the desired 50 Ω input matching. Note that there will be a small DC voltage drop across R_s that will consume headroom at the output, but the increased flexibility in the input matching design justifies the trade-off. The proposed T-matching network indeed provides third order isolation in the operating band along with improved noise performance and achieves good input matching over the 3.1-10.6 GHz band of interest.

2.3 The Current Reuse Techniques

An effective way to reduce the power consumedly by any circuit is employ current reuse techniques. Instead of using multiple individual stages, each of which is biased separately, stages are stacked on top of each other to reuse the current consumed by the other.

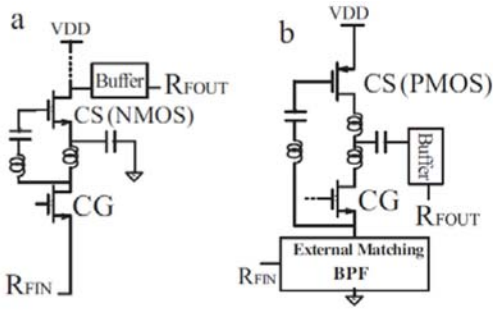


Figure 3. The current reuse architectures

In Figure 3, Architectures (a) and (b) can achieve the desired signal/noise phase difference at input without addition of extra components and to facilitate noise cancelling, however, due to large NF of pMOS, Figure 3 (a) is selected. To minimize the power dissipation, current reuse technique is employed by stacking up the CG nMOS and the CS nMOS amplifiers. A wideband, high gain and low power LNA is achieved through this architecture. The high gain is primarily a result of cascading of CG and CS amplifiers. Conventionally, M_1 and M_2 are connected as a cascade topology to design a noise cancelled UWB LNA. There are CG stage (M_1), which provides wide input impedance matching for the wideband and the CS stage (M_2), which provides the gain over the entire band. In Figure 2 (a). M_1 and M_2 are regarded as a cascade topology, which consumes the same current to operate each transistor at the same time. Some passive components are needed for the current reused structure.

2.4 The Stability Factor Analysis

Unlike the other circuits in a receiver, the LNA must interface with the "*outside world*," specifically, a poorly-controlled source impedance. For this reason, the LNA must remain stable for all source impedances at all frequencies. The stability of LNAs is an important requirement. The stability factor (K) is a popular measure of circuit stability. When K>1, the circuit will be unconditionally stable. When K<1 then circuit is potentially unstable and oscillation may occur with a certain combination of source and /or load impedance presented to the transistor. The value of K is obtained as follow:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{6}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{7}$$

2.5. The proposed UWB LNA circuit

The CG stage failed to provide enough gain at higher frequency which is the main unacceptable outcome for UWB applications. Thus, the design of the CG amplifier adopts a multilevel structure to improve the circuit performance. Figure 4 shows the schematic of the proposed UWB LNA. The design of the circuit also incorporates the T-matching network technique and the current reused technique, respectively. The first stage of the UWB LNA configuration consists of the CG input stage (M_1) for input wideband matching, the CG stage with low input impedance characteristic and broadband behavior, provides NF that is almost independent of the frequency of operation. The CG stage also eliminates the Miller effect and hence provides better isolation from the output return signal. To decouple the NF from the input matching condition and to reduce the noise floor. Then the CS second stage (M_2) for gain improvement followed by an output buffer (M_3, M_4) used to drive 50 Ω.

CG is a coupling capacitor, which provides a signal path between the CG (M_1) and CS (M_2) stages. C_b is a bypass capacitor, which blocks the AC signal into the source of M_2 and increase the AC gain of the CS stage. It functions as an *AC* ground at high frequency. L_D is a RF choke inductor, which prevents the AC signal from passing through using high impedance from the drain of M_1 to the drain of M_1 to the source of M_2. The values of L_D and C_b affect gain flatness in the design employing the stagger tuning technique. The peaking inductor L_C and the parasitic capacitances at the drain terminal of M_1 and the source terminal of M_2 were parallel resonant at the lower corner frequency (3.1GHz), while the peaking inductor L_C and C_{gs3} were series resonant at the upper corner frequency (10.6 GHz). Transistor M_3 acts as a buffer. It is connected to transistor M_4, which is a current source for M_3. In this

way, flat power gain, high power gain, flat and low noise factor were achieve.

LNA design involves trade-off among many of figure of merits, such as gain, noise, power dissipation, input matching, stability, and linearity. Because the trade-off between input matching and S21 (and *NF*), $(1/g_{m1})||R_s \approx 15.8\Omega$ was adopted in this work.

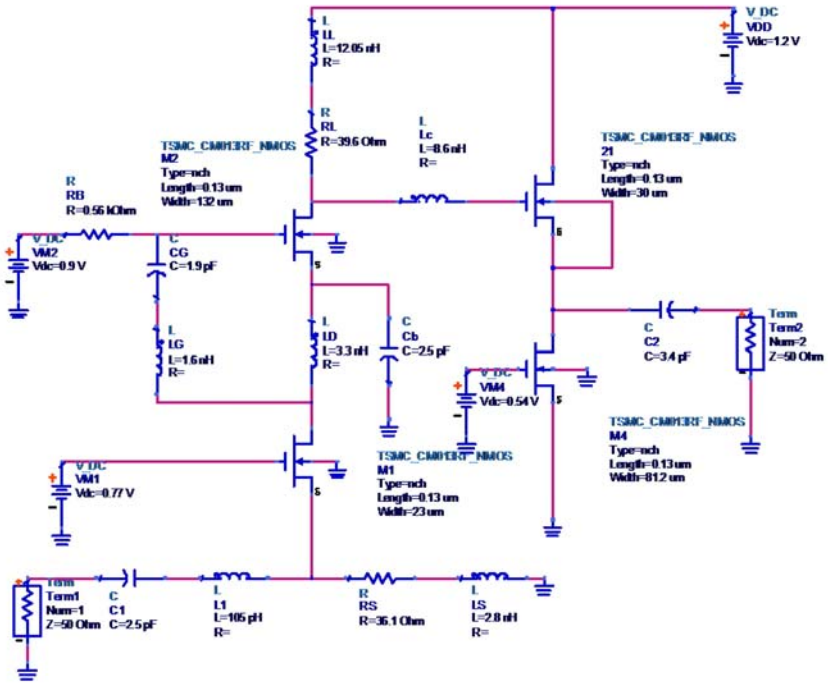


Figure 4.The Schematic of the proposed LNA

3. Simulation and Discussion

The designed circuit of Figure 4 is simulated with Agilent Advanced Design System (ADS) tools in TSMC 130 nm RF CMOS technology. *M*1, *M*2, *M*3 and *M*4 size are set to *W*1 = 23μm, *W*2 = 132μm, *W*3 = 30μm and *W*4 = 81.2μm. For input impedance matching network, L_1, R_S and L_S are set to 105 pH, 36.1Ω and 2.8 nH. C_G, L_G, L_D and L_C are set to 1.9 pF, 1.6 nH, 3.3nH and 8.6 nH.

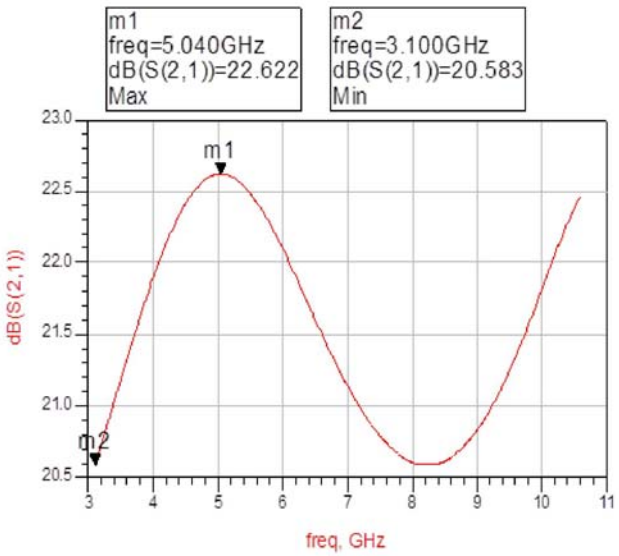


Figure 5. The Simulation results of power gain

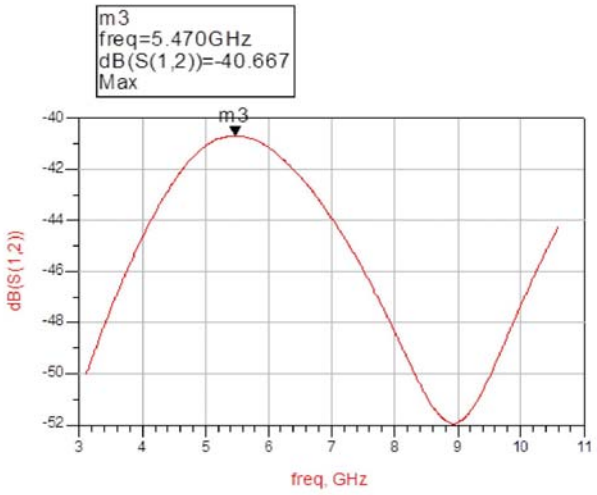


Figure 6. The Simulation results of reverse isolation

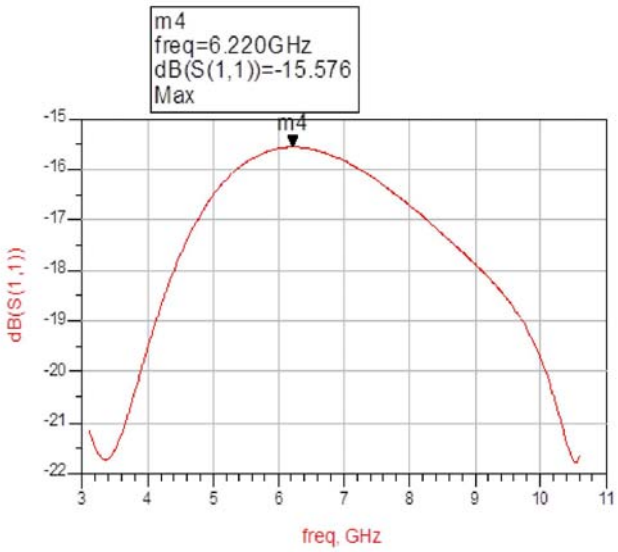


Figure 7. The Simulation results of input reflection coefficient

Figure 8. The Simulation results of output reflection coefficient

Results of S-parameters, noise and stable are shown in Figure 5 – Figure 10. Figure 5 shows the gain S21 is 21.603 ± 1.02 dB, maximum gain is 22.622 dB in band of interest, the flat gain can be achieved using the inter-stage matching at 3.1 GHz and 10.6 GHz. In Figure 6, S12 is below -40.667 dB due to RF chock inductor (L_D) and bypass capacitor (C_b) between transistor M_1 and M_2 within the required bandwidth. The better reverse S12 can reduce the latter local oscillation leakage arising from the capacitive paths and the substrate coupling. The value of input return loss (S11) is shown in Figure 7, the value of S11 is below -15.576 dB. Output return loss (S22) is less than -20 dB which are illustrated in Figure 8. Figure 9 clearly shows that the designed UWB LNA achieves a noise characteristic less than 3.22 dB from 3.1- 10.6 GHz which is a good candidate for wideband low noise application. Figure 10 shows the simulated K-factor of the UWB LNA. The UWB LNA which has the simulated K-factor over unity is unconditionally stable over the band of interest.

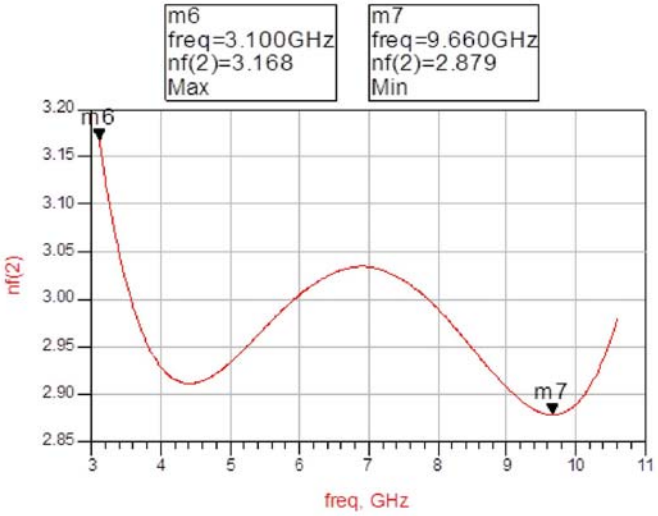


Figure 9. The Simulation results of noise factor

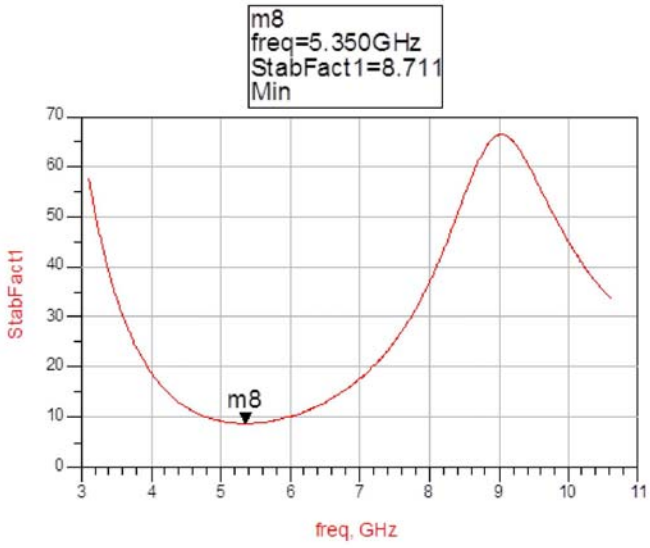


Figure 10. The Simulation results of stability factor

A comparison of our proposed LNA with other recently published LNAs is presented in Table 1. The FOM is also included in the table and defined in Equation (8) [16].

$$FOM = \frac{|S_{21}| * BW}{(|NF| - 1) * P_D} \quad (8)$$

Where |S21| indicates the average power/voltage gain, BW indicate the bandwidth in GHz, |*NF*| represents the average noise figure and P_D represents the power dissipation in milliwatts (mW). The proposed architecture achieves considerably high FOM compared to most of the recently published popular designs.

	Ourwork	[2]	[3]	[17]	[18]	[19]	[20]
Technology(nm)	130	130	130	130	180	130	180
BW(GHz)	3.1-10.6	3.1-10.6	3-10	2.35-9.37	3.1-10.6	0-11	3-10
S11(dB)(max)	-15.576	-5	-14	-8	-10	-11	-10
S21(dB)	22.622	21	17	10.3	12.6	20.5	21.35
S22(dB)(max)	-20.228	10.6	-5	-8	-10	-18	-10
NFmin(dB)	2.879	1	4.8	3.68	2.9	6.5	2.59
PD(mW)	5.82	4.1	13	9.97	15.2	9.36	33
FOM(GHz/mW)	13.76	14.56	2.29	5.71	1.8	3.59	2.45

Table 1. The Comparison of the simulated results of the proposed LNA with other recently published

4. Conclusion and Summary

In this paper, a high gain and low noise UWB LNA was proposed and evaluated for 3.1-10.6 GHz applications using TSMC 130 nm RF CMOS technology. The proposed UWB LNA was designed using T-match input network to improve the input matching at low frequencies and with the current reused technique to reduce the power consumption. It complies with the critical requirements of low noise performance with adequate power gain and linearity, as well as, effective input matching within the operating band along with low power dissipation. Simulation results show the gain was 20.583-22.622dB, S11 < -15.576 dB, S12 < - 40.667 dB, S22 < -20.228 dB and the noise factor was less than 3.168 dB. The total power was 5.82 dB including the output buffer with a 1.2 V power supply. The results indicate that this proposed LNA has a very good gain flatness and wide band flat noise performance.

Acknowledgments

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