A 65 - NM CMOS RF Mixer for Different Applications

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ABSTRACT: *A down conversion RF mixer is designed with 65nm CMOS technology for a different low power consumption applications. Mixer structure comprises a double-balanced Gilbert-Cell with improving linearity method in the RF stage of circuit; all is at a supply voltage of 1.8V and a power of 2.17 mW. The circuit is simulated for different spectrum applications as: 200 MHz mobile users, 1.9 GHz wireless applications, and 20 to 60 GHz commercial satellite and pointto- point communications. The reported design achieves good values in terms of a radio frequency mixer evaluating parameters such as: Consumed Power, Conversion Gain, Noise Figure and Linearity.*

Keywords: Component, Gilbert-Cell, Power Consumption, Linearity, RF Applications, 65NM technology

Received: 18 July 2014, Revised 28 August 2014, Accepted 31 August 2014

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1. Introduction:

At any RF channel; Mixer block has a critical impact on the performances of all system function; It is a non-linear device used to translate one frequency to another (*Figure. 1*). For a receiver chain (which concerns the present work) the local oscillator (LO) will drives by (switching/modulating) the incoming radio frequency (RF) to an intermediate low frequency (IF) [1].

It is within this context the work outlined in this paper. In sum, the goal is not only to design in 65nm CMOS technology an RF Mixer to improve the integration of circuit, with improving linearity process, or to measure the constraints associated to the nonlinearity, noise and the power consumption of design, but especially to simulate design and show its feasibility in several frequency bands for diverse applications, than compare its performances with recent works for each RF range.

2. Theoretical Performances And Feasibility

2.1 Circuit Design

RF signal is applied to the transistors (M2 & M3) (Figure 2), which perform a voltage to current conversion. MOSFETs M4 to M7 multiplie this current with local oscillator (LO) signal applied across M4 to M7 [2].

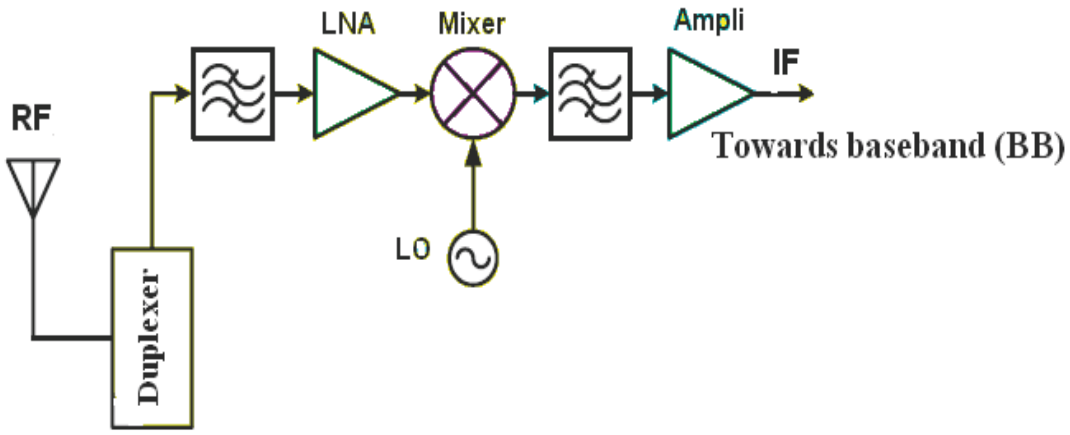

Figure 1. Typical transceiver block diagram

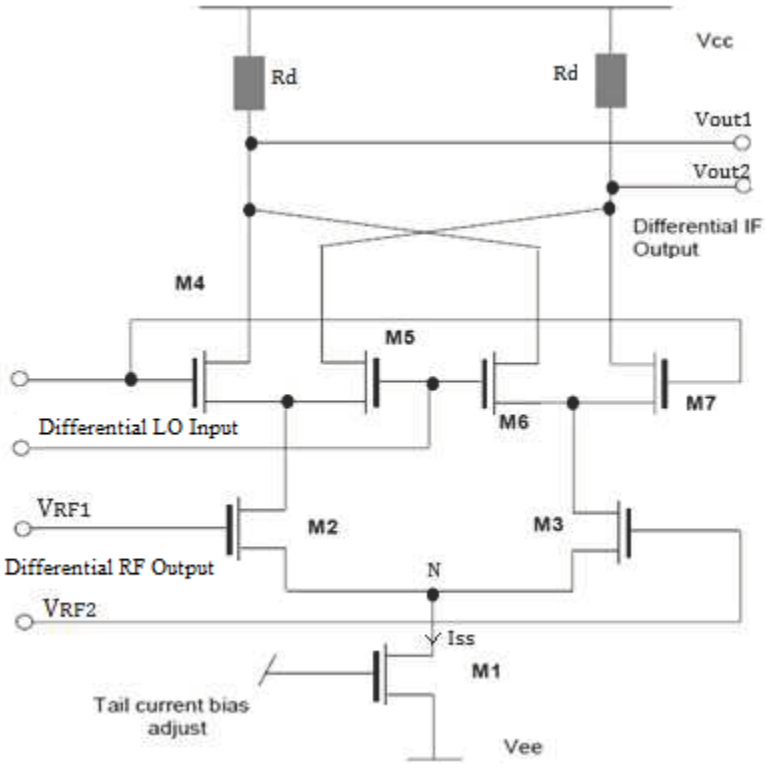

Figure 2. The used Gilbert-cell architecture

2.2 Good Trend Between Gain and Linearity

Following a theoretical analysis in our recent work [3] on which our objective was to find a linear variation of drain current ID relative to the input signal VRF without reducing the Gain of Circuit (Figure. 2), then conflicting to evaluating parameters of circuit.

Since the amplitude of RF signal stems from LNA block on RF chain, an (RL) degeneration circuit was proposed to increase the value of third order interception point (IIP3) without influencing the gain (Figure 3).

2.3 Work Objectives

In this paper, the main objective is to show the feasibility of the designed circuit within a wide margin of frequency [5] as:

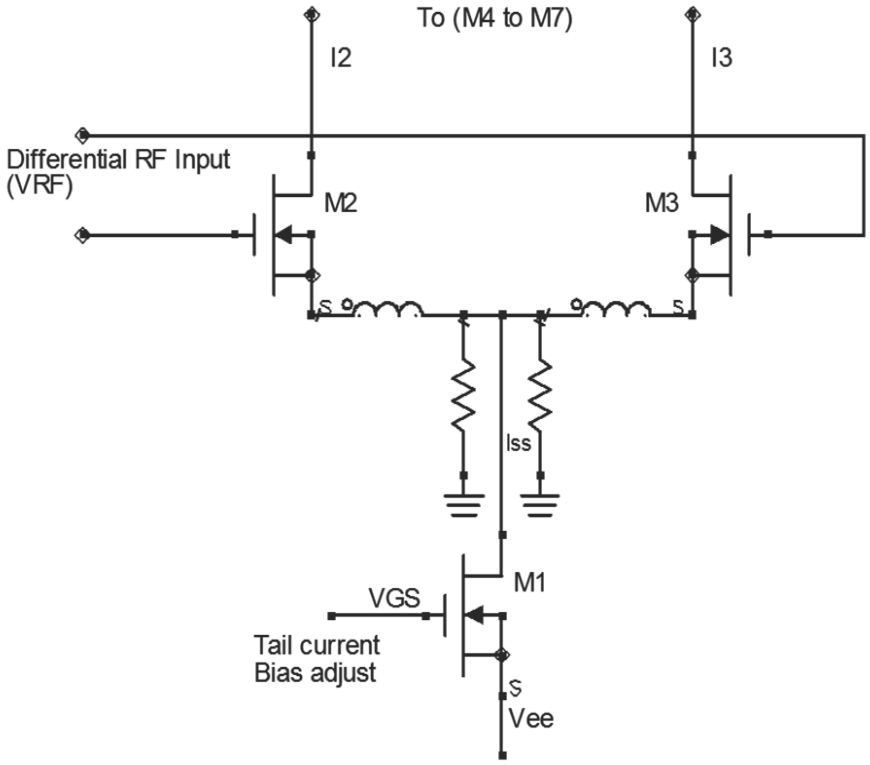

Figure 3. Proposed RL degeneration [3]

• **VHF** (Very High Frequency): between 30 and 300 MHz, this margin contains a large number of mobile user, radio taxis, familiar VHF FM broadcasts…

• **UHF** (Ultra High Frequency): between 300 and 3000 MHz, most of the terrestrial television stations are located here, and more mobile users including cellular telephones.

• **SHF & EHF** (Super High Frequency and Extremely High Frequency): above these portions of spectrums, there are many uses for radio spectrums, commercial satellite and point-to-point communications. SHF is from 3000 to 30000 MHz and EHF is from 30000 to 300000 MHz.

3. Simulation Results

On ADS tool, the choice of the MOSFETs length channel (65nm) was to maximize gain, to minimize noise and to optimize the footprint of circuit. The bias voltage of MOSFETs is Vdd = 1.8V.

The same design is simulated for each frequency range (200 MHz, 1.9, 20, and 60 GHz), which is dedicated to diverse RF applications. The following figures show: Harmonic Responses (Figure 5, Figure 8, Figure 11, and Figure 14) of the Output spectrums (the VRF amplitude remains the same in all selected RF bands and equal to -23.098dB (Figure 4). Linearity is represented by giving the third order interception point (IIP3) as shown in curves (Figure 6, Figure 9, Figure 12 and Figure 15), the present structure comprises an IIP3 equal to 3.5 dBm at 200 MHz chosen frequency for VHF applications, 11.6 dBm at 1.9 GHz UHF, 1 dBm at 20 GHz SHF, and 5.5 dBm at 60 GHz EHF. Based on the Input/ Output noise curves (Figure 7, Figure 10, Figure 13, and Figure 16) and the extracted Conversion Gain from RF and IF spectrums as shown in figures (Figure 5, Figure 8, Figure 11, and Figure 14), the noise figure is respectively equal to 6.26, 4.12, 10.23, and 10.24 dB in VHF, UHF, SHF and EHF.

Respectively for VHF, UHF, SHF and EHF, simulated performances of proposed design; are summarized in tables: Table I, Table II, Table III and Table IV, and compared with the most recent approaches, including Razavi typical characteristics of RF Mixer [6], our latest published works [3], [10], [11] and [12], also with a simulation results of LNAMixer architecture as [7].

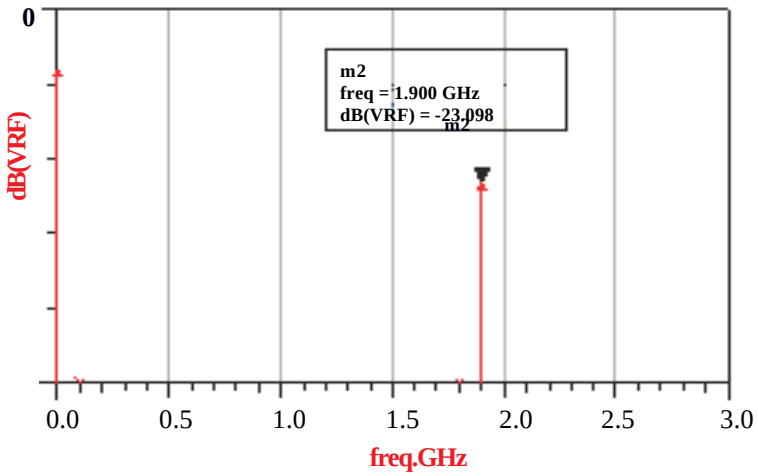

Figure 4. Frequency Input spectrum at fRF = 1.9 GHz example

GC (dB)	This work[a]	[8] [a]	[9] [b]	[6] [c]
GC (dB)	**9.85**	34	21	10
IIP3(dBm)	**3.5**	4	12.5	5
Power (mW)	**2.17**	3	67	—
NF(dB)	**6.26**	10	3	12
Frequency	**200 MHz**	402 -405MHz	200MHz-2GHz	—
Technology	**65**	130	65	—

Table 1. Summary result and performance comparison in VHF

[a] simulation results [b] values are raised from simulation curves [c] typical characteristics (B.Razavi, 1998)[6]

A. VHF, fRF= 200 MHz and fLO=190 MHz (broadcasting, biomedical telemetry…)

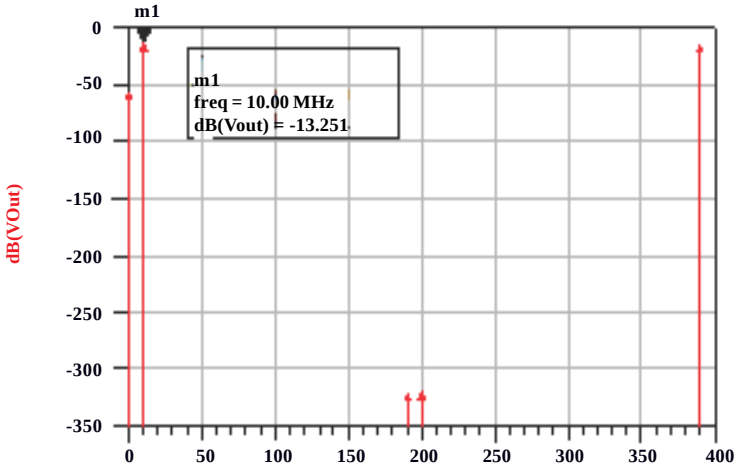

Figure 5. Frequency Output spectrum at fRF=200 MHz

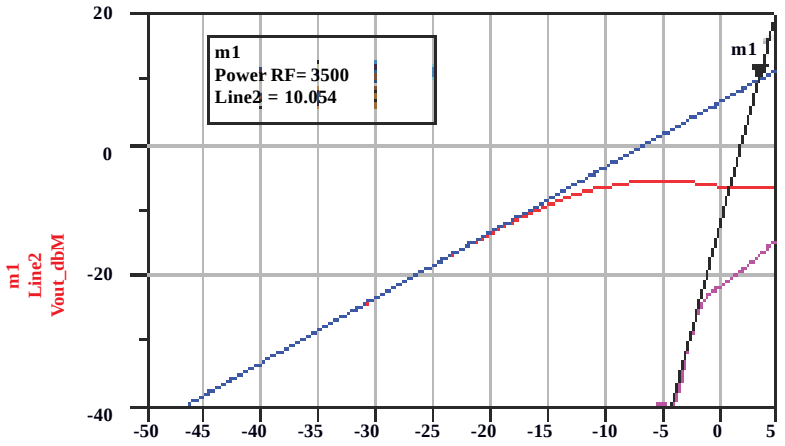

Figure 6. Third order interception point (IIP3) (fRF=200MHz)

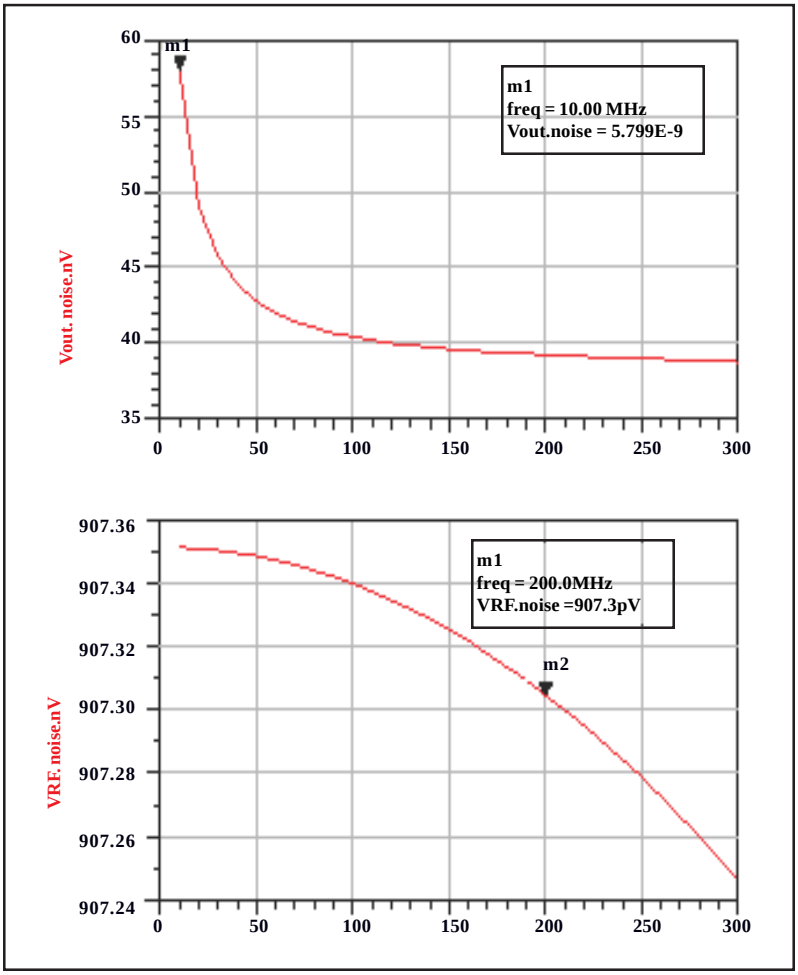

Figure 7. Input /Output noise (fRF=200MHz)

Compared to the approaches found (Table 1) and referring to typical characteristics [6], this circuit presents a very low power consumption, a miniaturized technology, a low noise and a good trade between linearity (IIP3) and gain (GC).

B. UHF: fRF = 1.9 GHz and fLO =1.8 GHz (GSM Wireless Applications)

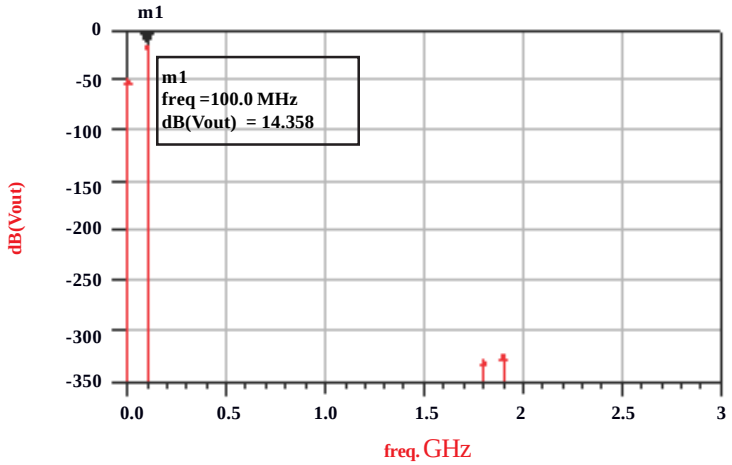

Figure 8. Frequency Output spectrum at 1.9 GHz

	This work	[10] [a]	[11] [a]	[12] [a]	[13] [a]	[14] [a]	[7] [b]	[6] [c]	[15] [a]	[16] [a]
GC (dB)	8.75	13.9	9.12	12.4	5.3	13	22.3	10	8.6	17.5
IIP3(dBm)	11.6	1.7	10.4	6	3.9	-3.08	-10.8	5	6.7	-7.2
Power (mW)	2.17	2.02	30.7	2.02	3.5	0.48	0.90	—	0.42	—
NF (dB)	4.12	3.13	9.74	8.92	19.4	12.7	7.2	12	19.2	13.5
Tech	65 *nm*	65 *nm*	0.18 *um*	65n *m*	0.18 *um*	0.13 *um*	0.13 *um*	—	0.11 *um*	0.13 *um*
Freq(GHz)	19	1.9	1.9	1.9	2.4	25	2.4	—	2.4	2.1

[a]simulation results, [b]simulation results of LNA-Mixer architecture
[c]typical characteristics (B. Razavi, 1998)[6]

Table 2. Summary result and performance comparison in UHF

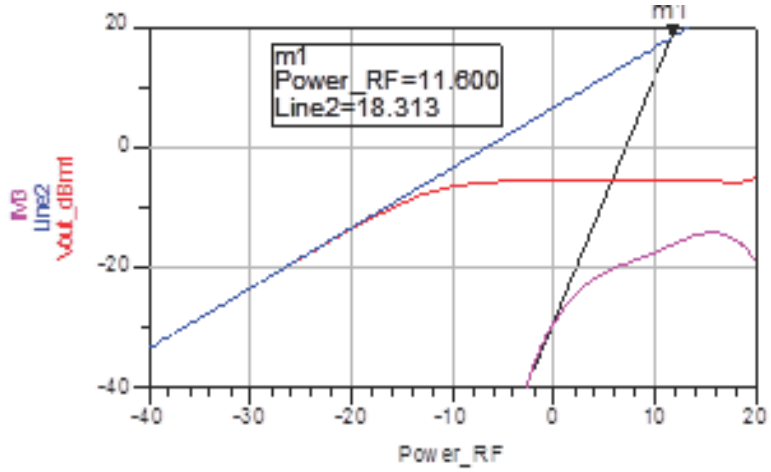

Figure 9. Third order interception point (IIP3) (fRF=1.9 GHz)

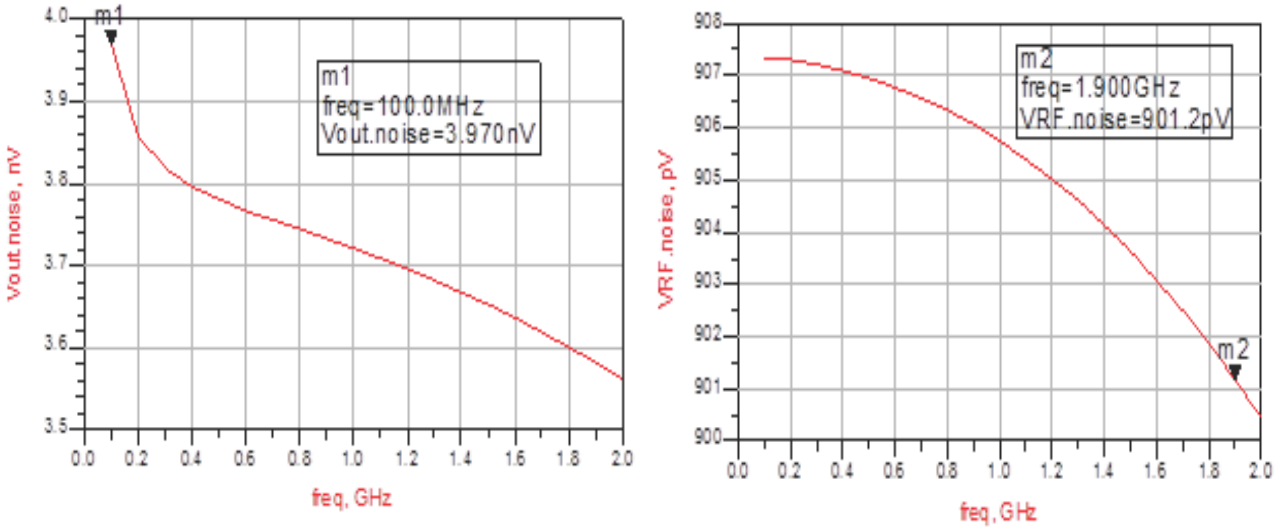

Figure 10. Input /Output noise (fRF=1.9 GHz)

C. SHF: fRF = 20 GHz and fLO = 19.9 GHz (Fixed Service Satellite)

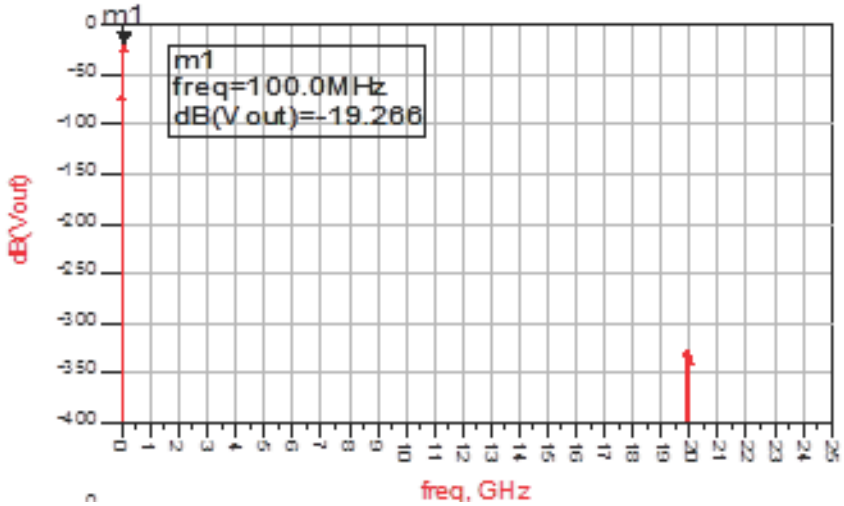

Figure 11. Frequency Output spectrum at 20 GHz

As shown in Table 2 for UHF band, the present work achieves a very low consumed power, a miniaturized technology, an acceptable Gain (CG), a low noise (NF), and a good linearity (IIP3).

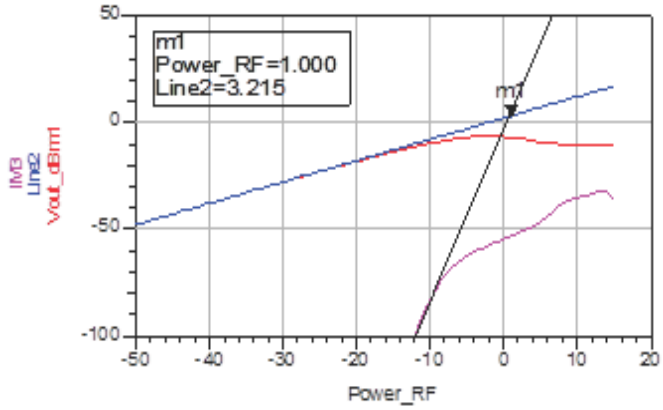

Figure 12. Third Order Interception Point (IIP3) (fRF=20 GHz)

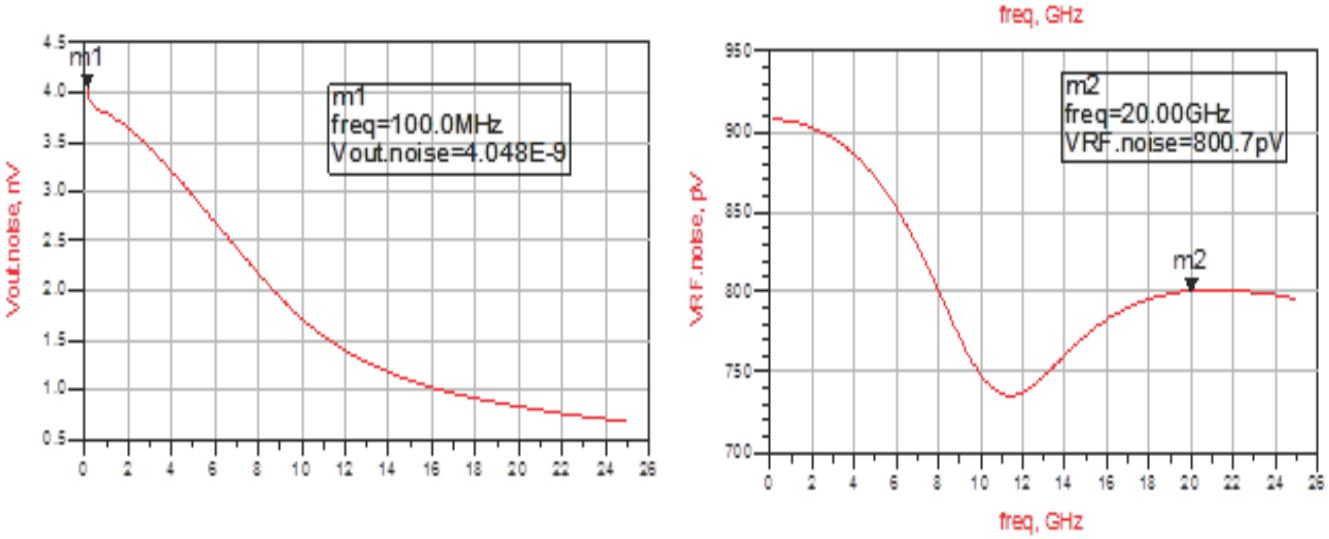

Figure 13. Input /Output Noise (RF=20 GHz)

	This work[a]	[17][a]	[18][a]	[6][b]
GC (dB)	**3.83**	16.32	<18.5	10
IIP3 (dBm)	**1**	3	8.5	5
Power (mW)	**2.17**	860	—	—
NF (dB)	**10.23**	14-16	—	12
Frequency (GHz)	**20**	6-20	24-31	—
Technology	**65nm**	200nm	500 nm G-FET	—
	CMOS	Bicmos		

Table 3. Summary result and performance comparison in SHF

From table 3, the present design is performing well in term of power consumption, a miniaturized technology, and the level of IIP3 is still acceptable.

D. EHF: fRF = 60 GHz and fLO = 59.9 GHz (Aeronautics, Space researches)

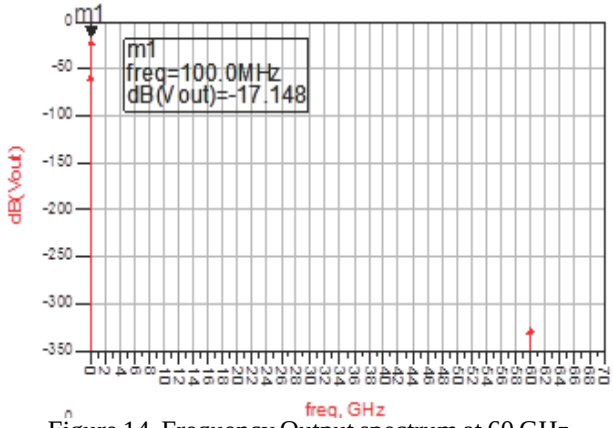

Figure 14. Frequency Output spectrum at 60 GHz

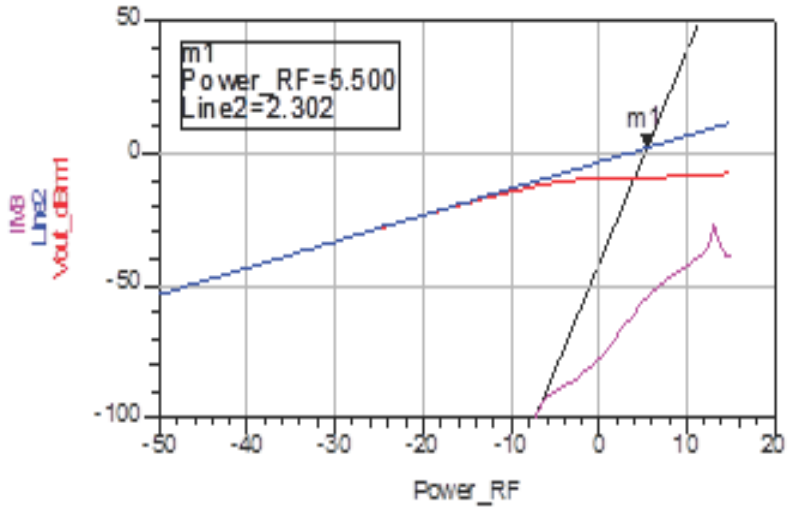

Figure 15. Third order interception point (IIP3) (fRF=60 GHz)

	This work[a]	[6][b]	[19][c]	[20][c]
GC (dB)	**5.95**	10	4	7
IIP3 (dBm)	**5.5**	5	—	-4
Power (mW)	**2.17**	—	13.6	0.453
NF (dB)	**10.24**	12	20	14.25
Frequency (GHz)	**60**	—	75	60
CMOS Technology (nm)	**65**	—	90	90

[a] simulation results, [b] typical characteristics, [c] values are raised from simulation curves
Table 4. Performances comparison at EHF

According to presented data (*Table 4*), this circuit achieves a good values in terms of linearity (IIP3), the power consumption is acceptable, a very good value of noise figure and an acceptable conversion gain (CG).

4. Conclusion

Simulation results highlight the potential applications of the proposed mixer architecture in a different higher frequency communication systems, the most important parameters characterizing an RF mixer are extracted, and compared to the approaches found recently, this circuit presents a very low power consumption, low noise, good linearity, a miniaturized CMOS technology and an acceptable conversion gain. That shows the performance of this choice compared to recent technologies for each portion of RF spectrums. Current-Driven Subharmonic Mixer in 0.13 CMOS, IEEE *Transactions on Circuits and Systems-I*, 60 (5).

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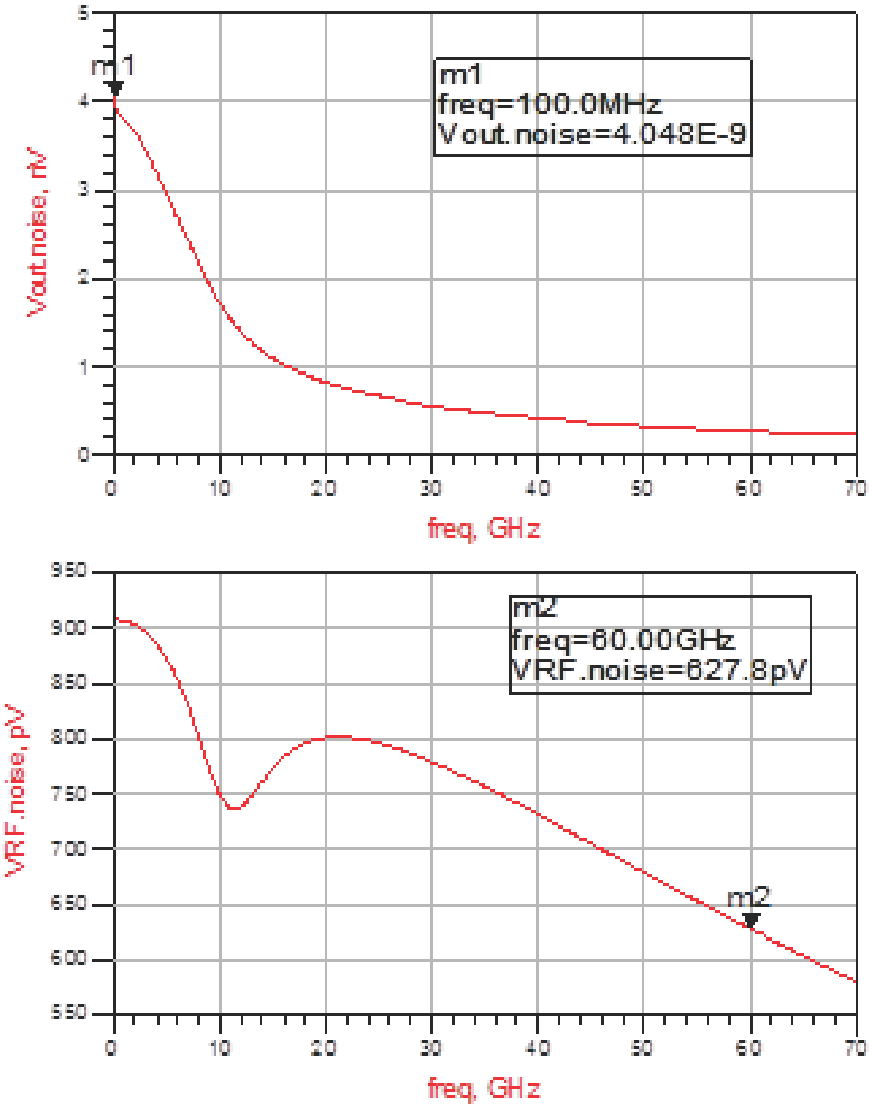

Figure 16. Input /output noise (fRF=60 GHz)

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