Editorial

We present the first issue of this **Electronic Devices** volume with the papers below.

In the opening paper, "**A study of bus contention in FPGA framework,"** the authors studied the maximum bus contention encountered by hardware accelerators functioning within the FPGA framework. They started the study with a comprehensive model of the AXI bus and its interconnections. Next, contention delays are examined within hierarchical bus architectures of different levels. Finally, they presented experimental results to validate the proposed model.

In the second paper, "**Analysis of the topology in radio networks using undirected connected graphs,"** the authors addressed the challenges in ascertaining the size and identifying the topology in radio networks represented by basic undirected connected graphs. They measure the size required that every node reports the total count of nodes in the graph, which is its size. To assist, they developed an algorithm which operates within a time complexity.

In the last paper, "**Lazy Backtracking Model for Incremental Inquiries and Re-implication Strategy,"** the authors studied a novel open-source CDCL SAT solver. They used the Lazy Backtracking method to allow significant properties to be regained to compensate for the lost solvers.

We hope that these papers generated significant interest among readers.

Editors