Editorial

We present the third issue of **Electronic Devices**, featuring the following papers.

In the first paper, "**A Federated Framework of Multiprocessor Scheduling for Real-time Tasks**," the authors introduce a model for efficiently depicting parallelizable real-time tasks. This model defines each task using a handful of parameters acquired through multiple executions of the code under varying conditions. This process enhanced the effectiveness of the federated framework for multiprocessor scheduling.

In the second paper, "**A Methodology for Generating Representative Benchmarks for Machine Learning-Driven Code Optimization," the authors outlined** a methodology for generating representative benchmarks to evaluate source-to-source code transformations using machine learning (ML). The proposed model supports active learning to select the most informative samples, improving ML model efficiency with less labeling effort.

In the last paper, '**Multithreaded FPGA Accelerators via Dataflow Modeling with Token Tagging," the authors** presented a novel model-based approach for designing multithreaded hardware accelerators on FPGAs using a dataflow paradigm. The approach is validated using a video coding use case involving HEVC fractional pixel interpolation, implemented in two versions (Baseline and Matrix). This work demonstrated the feasibility of dataflow-based multithreading for FPGA accelerators, with future goals including OS.

We hope that these papers generate interest among readers.

Editors