3D Microelectronics: Teaching Experience and Research Promising Field

Abir M'zah, Omar Hammami
ENSTA ParisTech
32 Bvd Victor
75015 Paris, France
{abir.mzah, omar.hammami}@ensta-paristech.fr

ABSTRACT: *3D Design is not really a new technology; in fact the first ASIC design was designed in 1986. These last years, the interest in 3D is emerging to deal with the problem of the interconnect delay which is overcoming the gates delay in nanometer technologies. 3D ASIC design is facing industrial and academic challenges. We present in this work, the description of a 3D ASIC designs practical work teaching to students applying to the Master degree.*

Keywords: Component, 3D Design, ASIC, Challenges, Teaching

Received: 19 August 2012, Revised 10 October 2012, Accepted 14 October 2012

1. Introduction

Some consider that CMOS scaling issue is reaching its limitation in face of the semi conductor physical properties in the nanometer scale. Moreover, with a nanometer CMOS technology, the link delay is becoming more important than the gates delay [1]. To deal with these 2 limitations, 3D conception can be the new solution allowing short vertical connections and smaller design area which facilitates its integration in small microelectronics devices [2]. 3D design is an emerging technology in the industrial and the academic domains. In fact, we can be easily convinced about the advantages of the 3D design compared to an equivalent one in 2D: smaller form factor, shorter connections, lower power consumption, and higher frequency. But few people are making a real 3D design implementation. 3D technology is facing a big problem which is the shortage of the 3D specific tools. We present in this work our experience in teaching a practical work based on the 3D methodology provided by Tezzaron technology. This course was targeting students having the master level degree. We will detail in section II the step of preparation. Section III will be the subject of the time management. We will present in section IV the student's evaluation. We will then conclude in the last section.

2. Preparation: Tools Exemples and Documentation

The practical work is a related to the theoretical course based on Multi Processor System On Chip. The first step of the preparation is to analyze the background of the group of the students. We notice that the students have different basic formations. There is even some who has only a basic level in Microelectronics. This factor can have a meaningful effect on the preparation of the practical work. The majority of the students have a good theoretical knowledge about Cadence tools and 3D Technology. This practical work should be an application to the magisterial course which is about MPSOC. That is why; students should ideally implement a 3D MPSOC architecture. We propose to use in this course, an open core processor called

OpenFire presented in Figure 1. We choose to use this processor to encourage the students to find the needed information by themselves. This processor was the subject of a PHD which represents a good documentation support to have a detailed description of the processor.

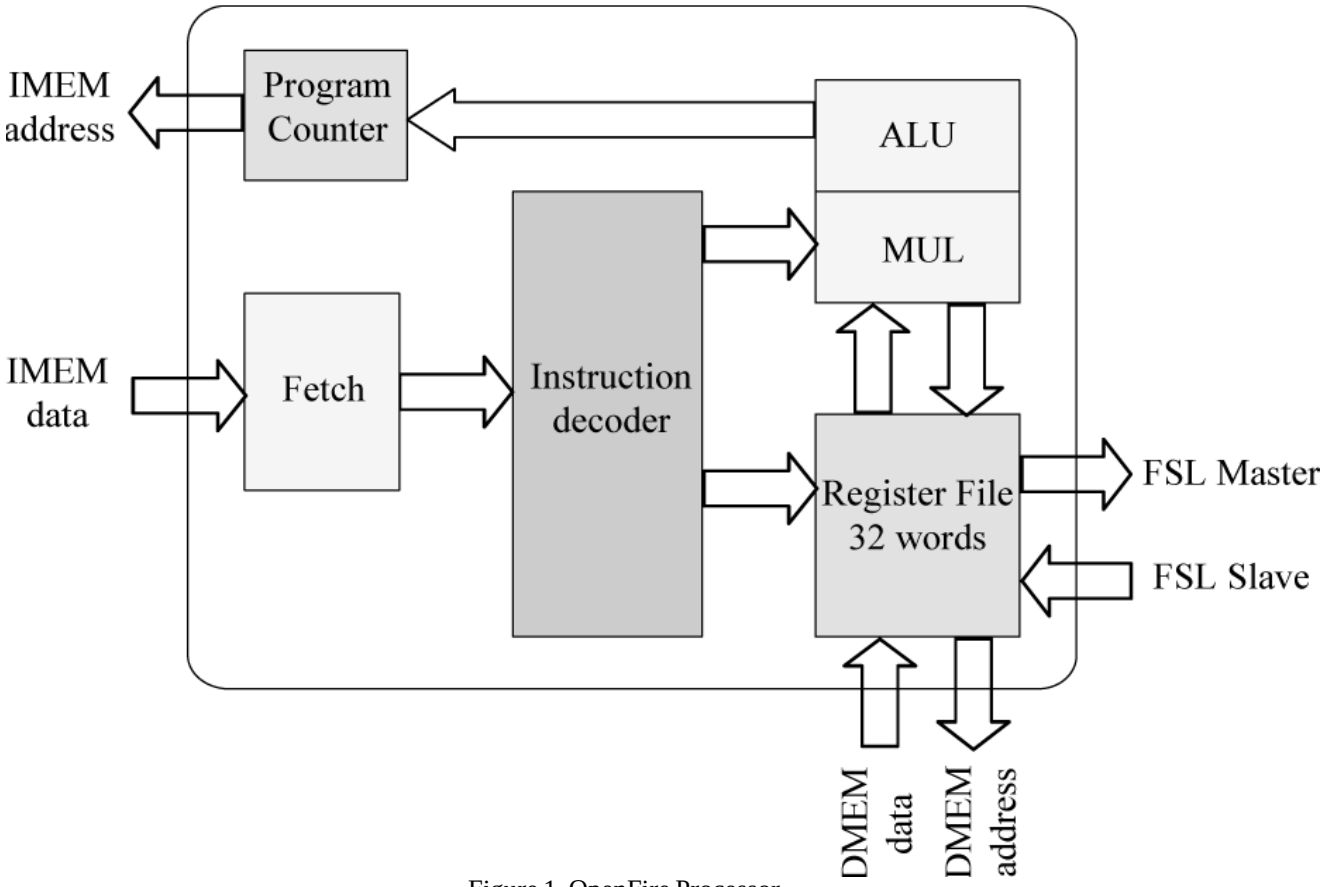

Figure 1. OpenFire Processor

Thanks to the previous information we prepare 2 basic documents. The first one is defining all the steps of a classical 2D Design implementation. A step by step example is provided to help the student to implement the first simple design. The second document is describing the 3D project to be realized by the group of students. Each group should implement a 3D architecture based on the openfire processor and using Tezzaron [3] technology. We prepare a folder containing all the scripts needed to implement the first guided example to be provided to the students. All the needed tools (Cadence, MentorGraphics, and Tezzaron) are installed in a classroom to be used during the practical work.

3. Teaching and Objectives

The major constraint of this course is the time. In fact students can only use the tools during the classroom time. Students should make the conception of a 3D architecture based on the Openfire processor. We present in Figure 2, the 3D ASIC design workflow. The student will use 4 basic tools: Modelsim, RTL Compiler, SoC Encounter and Virtuoso. The whole time reserved for the practical work is 6 hours (1H30 x 4). We present in TABLE 1, the planning of the time during this course. As we have a restricted access to the tools and in order to maximize the productivity, students should be interactive and prepare the projects before the classroom time.

The student should master at the end of the course the 3D workflow. He should be able to implement an MPSOC including the Openfire core using the 3D Tezzaron technology. The architecture of the processor and the 3D theoretical aspects should be also mastered.

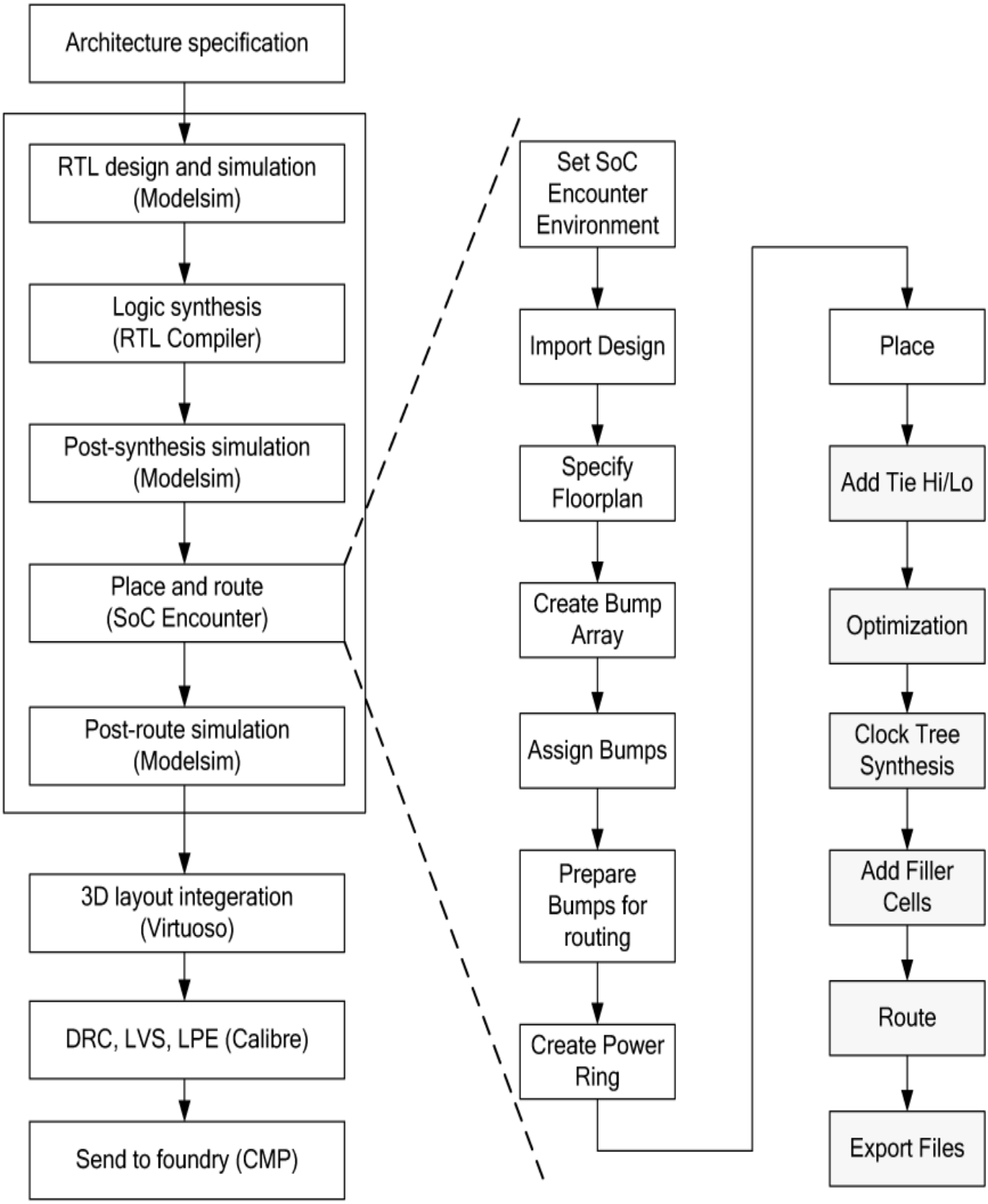

Figure 2. Tezzaron Design flow

Time	Task
1H30	• Tutorial 1 : Example ALU 2D ASIC Design • Simulation : Modelsim • RTL Compiler : RTL synthesis, • SoC Encounter : floorplan, place and route
1H30	• 3D presentation • Tutorial 2 : 3D Example implementation with Tezzaron technology (Automatic Script)
Extra Time	• Download the VHDL code of the Openfire Processor • Master the Architecture to be implemented • Prepare the VHDL MPSOC Architecture • Prepare the modified scripts (RTL synthesis, SoC encounter) • Interaction professor -students by e-mail
1H30	• Simulate the 3D Design • Implement the 3D Design
Extra Time	• Prepare the VHDL MPSOC Architecture • Prepare the modified scripts (RTL synthesis, SoC encounter)
1H30	• Interaction professor -students by e-mail 1H30 • Simulate the 3D Design • Implement the 3D Design

Table 1. Teaching Time Planning

4. Results and Evaluation

The students present the achieved results of the 3D MPSOC implementation. Students are divided into 2 groups to propose different works. Within each team, the main tasks are: simulation, Optimization, Layer 1 implementation and layer 2 implementation. We present in Figure 3 an example of an achieved result by a group of students. They present the result of simulation, synthesis logic and implementation.

5. Results and Evaluation

We presented in this paper an example of 3D course given to master degree students. Even though all of them had 0% knowledge about the 3D technology and tools, we got at the end of the formation good results. This experience showed that even though 3D technology is an emerging technology, it can be taught to students having basic knowledge in basic Microelectronics.

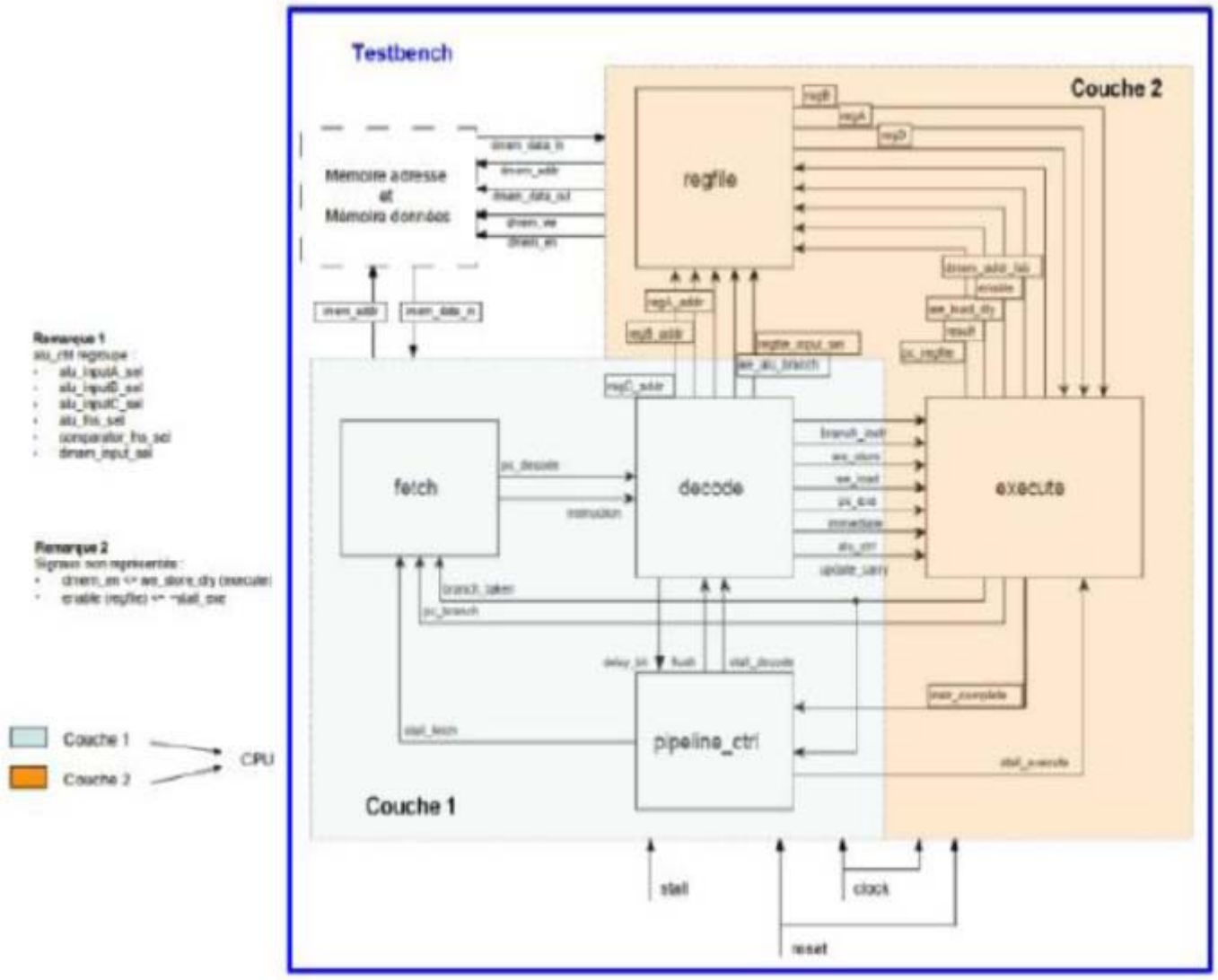

Figure 3. Example of realized project

References

[1] Robert, F., Jens, L., Tilo, M. (2009). From 3D circuit technologies and data structures to interconnect prediction, *In*: Proceedings of the 11th International workshop on System level interconnect prediction, ACM, San Francisco, CA, USA.

[2] Source: Nomura, K., Abe, K., Fujita, S., Kurosawa, S., Kageshima, A. (2010). Performance analysis of 3D-IC for multi-core processors in sub-65nm CMOS technologies, Circuits and Systems (ISCAS), *In*: Proceedings of 2010 IEEE International Symposium on, p. 2876-2879. 3D integration, *Microelectronics Reliability*, 50, p. 481-488.

[3] http:/opencores.org

[4] Ko, C.-T., Chen, K.-N. (2010). Wafer-level bonding/stacking technology for Microelectronics, *Reliability*, 50, 481-488.

[5] Tezzaron Design Kit CMP, http://cmp.imag.fr