# The Performance of Buck DC-DC Converter for Gate Driver with Adaptive Dead Time

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***ABSTRACT:*** *In the current work we studied the performance of the BUCK DC-DC converter with Zero Voltage Switching (ZVS). To test the object, we have advocated a simulation scheme of Gate Driver with Adaptive Dead Time. It enables the independence of ZVS from the current value at which the transistors are switched. We have simulated the influence on the switching losses of an externally connected drain-source capacitor. It is important to measure the mean value of the currents, the losses in transistors and the efficiency for which Macros in the graphical analyser is required. Trial data is obtained for testing the functions.*

**Keywords:** Power Electronics, Switch Mode Power Supply, Buck DC-DC Converters, Zero Voltage Switching

**Received:** 27 February 2021, Revised 9 May 2021, Accepted 5 June 2021

**DOI:** 10.6025/jes/2021/11/3/86-93



## 1. Introduction

The switched mode DC-DC converters are widely used to convert one level of electrical voltage into another level by switching action. These converters have received an increasing deal of interest in many areas, such as: cellular phones, tablets, laptops, radio-frequency power amplifiers, light emitting diode (LED) drivers, etc.

The most commonly used is the BUCK DC-DC converter with Pulse-Width Modulation. Recently, due to its better efficiency, the BUCK DC-DC converter with ZVS is approved. This type of control, with respect to their principle of operation, is similar to Hysteresis Current Mode Control (HCMC).

The BUCK DC-DC converter with HCMC and ZVS is characterized in that the lower hysteresis level has a minimum negative value and is a constant. The regulation of the output power is performed by changing the upper hysteresis level [1, 2]. The application of this control approach leads to optimal output-voltage transient response [3, 4] in addition to improving the efficiency.

A subject of the present paper is the construction of a simulation model of BUCK DC-DC converter with HCMC and ZVS, which allows efficiency investigation.

An example study is performed using Infineon's SPICE Model of the transistor BSC024NE2LS [5].

## 2. Buck DC-DC Converter with HCMC and ZVS

### 2.1. Power Circuit and Control System

The power circuit of the BUCK DC-DC converter is shown in Figure 1. The selected SPICE model for the transistors Qt (top) and Qb (bottom) allows the study to be performed depending on the crystal temperature of the transistors.

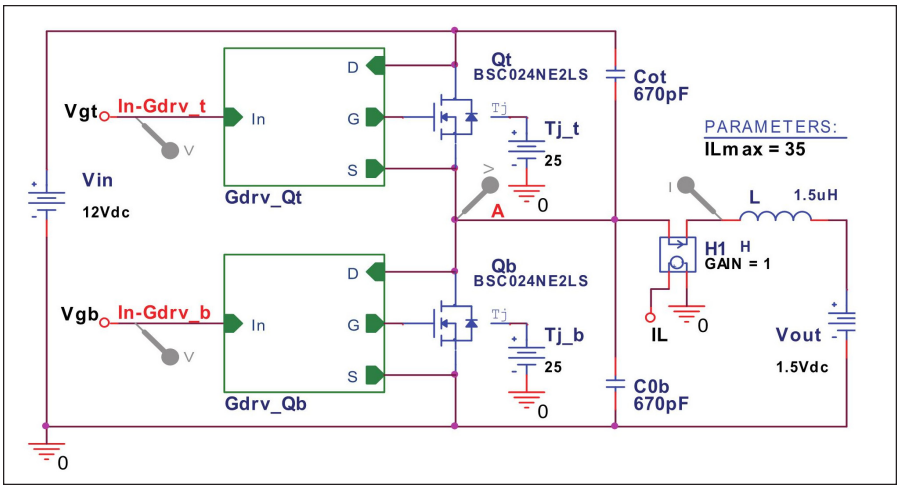


Figure 1. BUCK DC-DC Converter

The control system of the DC-DC converter with HCMC and ZVS is shown in Figure 2. Using the comparators EL (low level) and EH (high level), pulses are generated, corresponding to the Low and High Level of the current $I_L$ through the inductor $L$.

The comparator is realized by the Analog-Behavioral Model (ABM) element of EFREQ type using the function: 5*(sgn(V(% IN+, % IN-))+1)/2. The comparator EL sets the R-S trigger (U1, U2) in state "1" and as a result the transistor Qt is turn-on and the transistor Qb is turn-off.

The comparator EH sets the R-S trigger in state "0", whereby the transistor *Qt* is turn-off and the transistor *Qb* is turn-on.

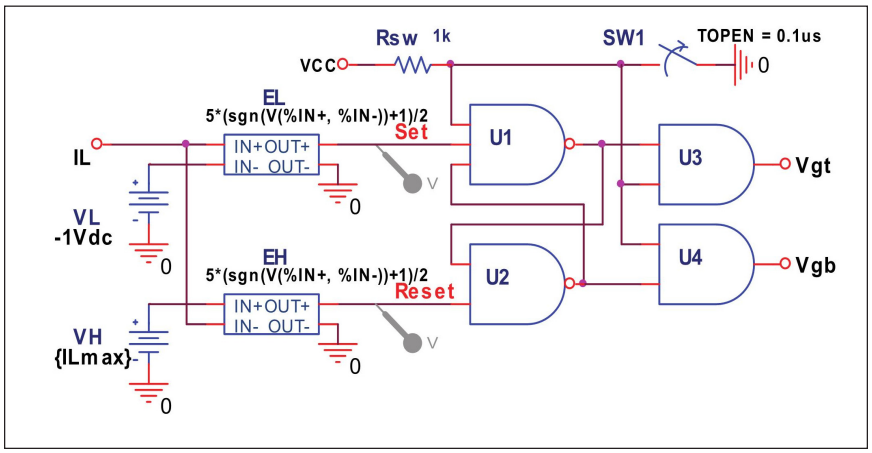


Figure 2. Hysteresis current mode control system

The principle of operating of the control system is illustrated by the waveforms shown in Figure 3.

The value $I_{L,\ LowLewel} = -1\text{A}$ is selected for the low level of the current $I_L$. The high level of the current $I_L$ is a simulation parameter and changes in the range from 2A to 35A.

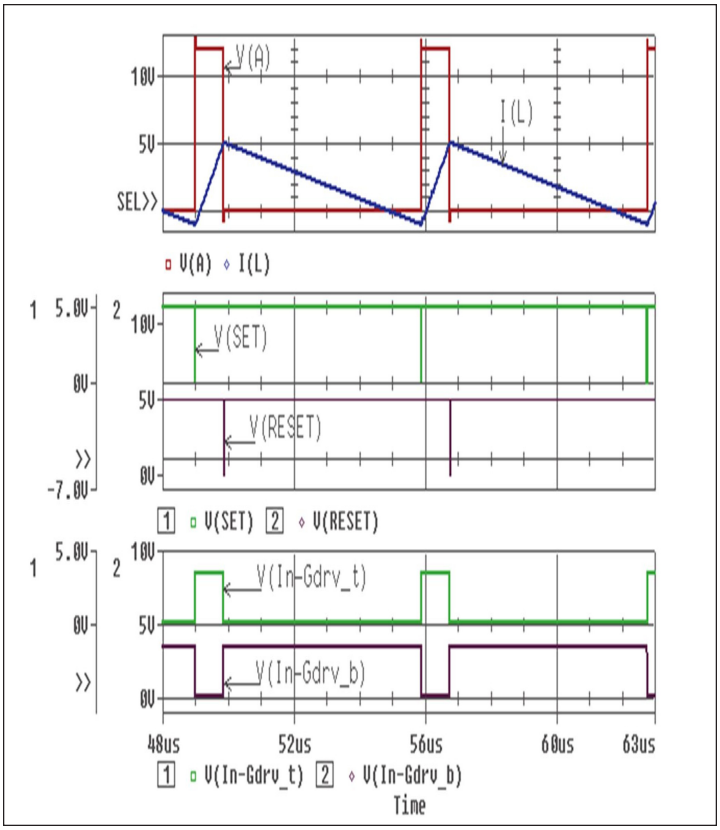


Figure 3. Waveforms illustrating the principle of operation of BUCK Converter with ZVS

In this case of HCMC, the switching frequency depends on the hysteresis window $\Delta_{IL}$ [6]:

$$f_{SW} = \frac{1}{L\Delta I_L} \cdot \frac{V_{out}\left(V_{in} - V_{out}\right)}{V_{in}}, \tag{1}$$

where

$$\Delta I_L = I_{L,HighLevel} - I_{L,LowLevel}.$$

**2.2. Gate Driver with Adaptive Dead Time**

In order for ZVS to be possible, it is necessary the transistor turn-on pulse $V_{gs}$ to be applied after the moment when the output capacitance of the MOSFET transistor is discharged by the current $I_L$ during the dead time (DT).

The duration of DT ($t_{DT}$) is a function of the instantaneous value of the current $I_{L,\ HighLevel}$. The Gate Driver scheme with adaptive dead time is shown in Figure 4. In this case, the index "*t*" corresponds to the top Gate Driver (for the bottom Gate Driver the index "*b*" is used).

Using the voltage-controlled switch *St*1 and the delay element *Ut*5, a comparator model is realized (with propagation time 10ns).

When the voltage $V_{ds}$ is less than 0.5V, the logical element Ut2 allows the applied pulse at the input *In* to reach the transistor's gate. The delay element Ut1 and the logical element Ut3 form a maximum value of $t_{DT\text{-}max}$. This value is needed by the starting the DC-DC converter, since then the current $I_L = 0$. The switches S1t and S2t represent a classical driver of two transistors (*n-p-n* and *p-n-p*).

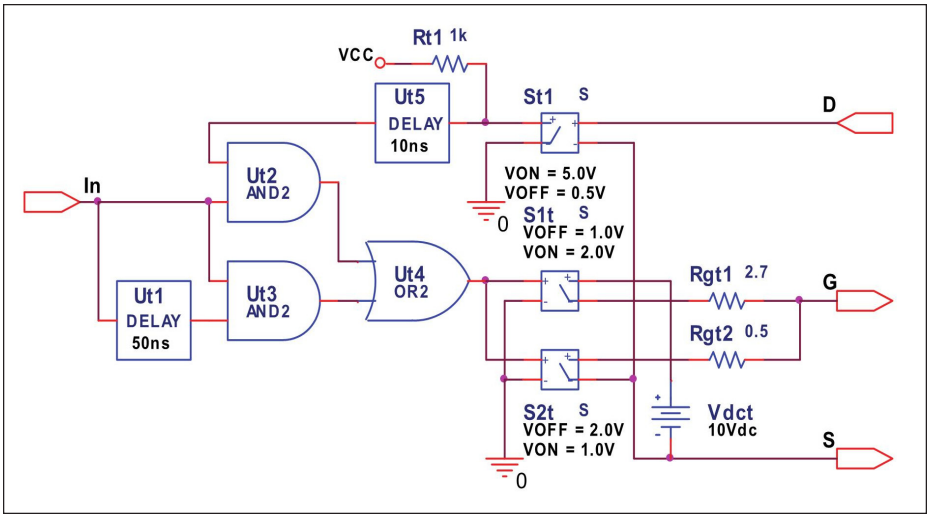


Figure 4. Gate Driver with Adaptive Dead Time

### 3. Simulation Results

The BUCK DC-DC converter with HCMC and ZVS is investigated using the program Cadence PSpice [7]. The simulation is performed for the time interval from 0 to 250 μs.

The following macro-definitions in the graphical analyzer *Probe* are defined for the post processing of the simulation results:

- The values of the currents and voltages in top and bottom power MOSFET transistors:

```
Id_b = I(Qb:DD)
Id_t = I(Qt:DD)
Vds_b = V(Qb:DD)
Vds_t = V(Qt:DD)-V(Qt:S0)
```

- The values of dissipated power in top and bottom power MOSFET transistors:

```
Pds_t=Vds_t*Id_t
Pds_b=Vds_b*Id_b
```

- The average value of dissipated power:

```
avg_Pds_b=max(S(M(Pds_b))/249us)
avg_Pds_t=max(S(M(Pds_t))/249us)
```

- The average value of the output current and output power:

```
Iout=YatX(AVG(I(L)), 250u)
Pout=1.5*Iout
```

- The efficiency:

```
efficiency=Pout/(Pout+avg_Pds_t+avg_Pds_b)
```

The macros thus defined can be reused.

The waveforms illustrating the ZVS transistor switching are presented in Figure 5 as follows:
– Figure 5*a* and Figure 5*c* – Qb-off, Qt-on (*IL* = –1A);
– Figure 5*b* and Figure 5*d* – Qt-off, Qb-on *(IL* = 35A);
– Figure 5*a* and Figure 5*b* – without additional capacitor drain-source (only with parasitic capacitance *Co* = 650pF of transistor BSC024NE2LS);
– Figure 5*c* and Figure 5*d* – with additional capacitors *Cot* = *Cob* = 670pF.

The switching losses *Pds-t* and *Pds-b* are presented on the coordinate systems (1) and (2). It is seen that the main switching losses are in the transistor Qt, at the moment of its turn-off, when the current $I_L$ = 35A. The additional capacitor $C_{ot}$ leads to a two-fold reduction of the amplitude of *Pds-t*, but at the expense of longer duration.

The input pulses *InGdrv_t* and *In-Gdrv_b* of the Gate Driver are shown on the coordinate system (3), plot 1 and the gate pulses *Vgs_t* and *Vgs_b* – on plot 2.

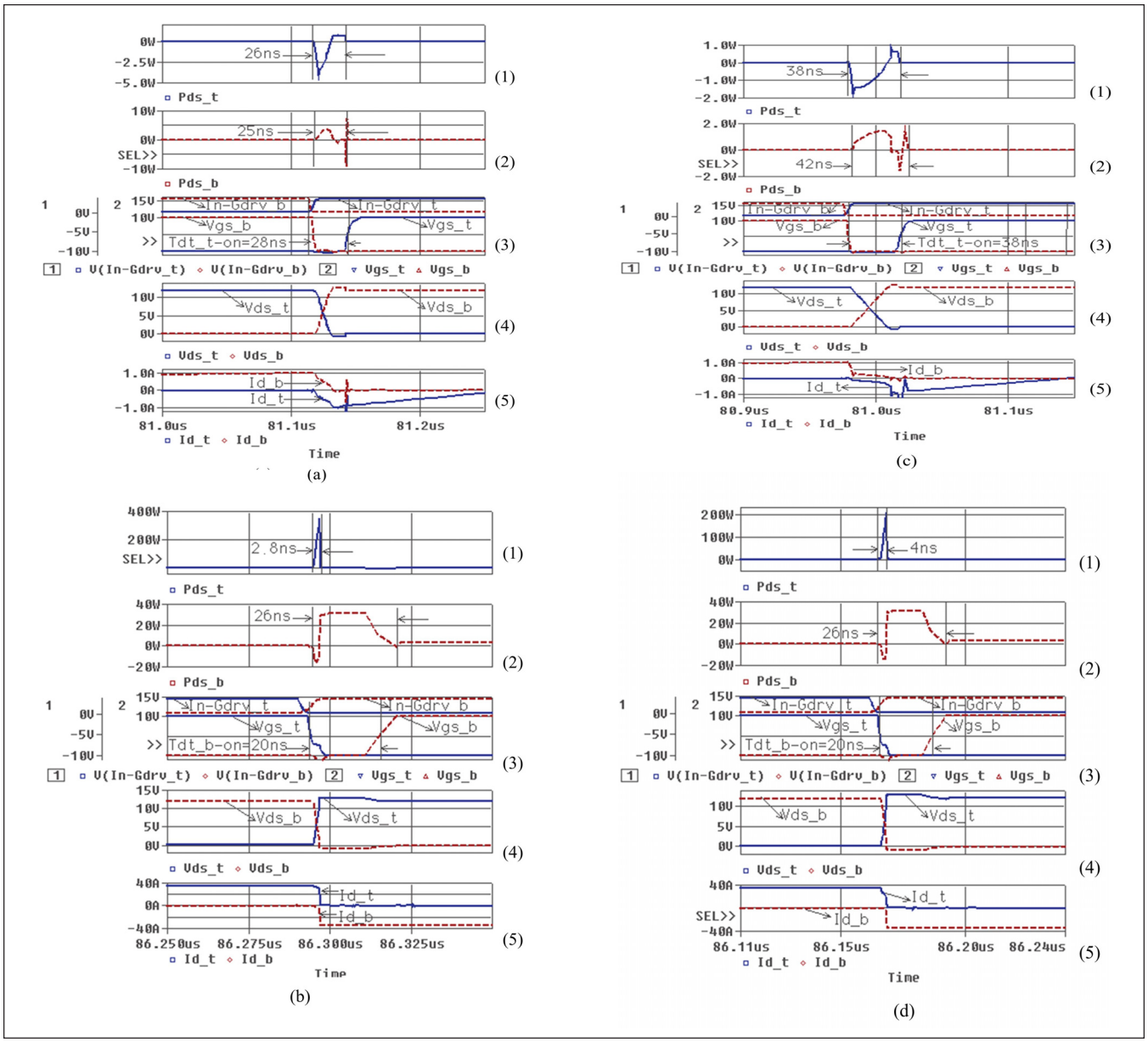


Figure 5. Waveforms illustrating ZVS processes by *IL-High Level* and *IL-Low level*

It is seen that the dead time for the transistor Qt increases twice when the additional capacitor $C_{ot}$ is connected. For the dead time for transistor Qb, there is no change when the additional capacitor $C_{ob}$ is connected, which can be explained by the large value of the switching current (at this time moment $I_L$ = 35A).

The voltages *Vds_t* and *Vds_b* are shown on the coordinate systems (4). The additional capacitor $C_{ot}$ leads to reducing the slope of the drain-source voltage.

By comparing the *Vds_t* and *Vds_b* waveforms with *Vgs_t* and *Vgs_b* waveforms from the coordinate system (3) – plot 2, it can be seen that the gate pulses reach the corresponding transistors when the drain-source voltage has become 0V. On the coordinate system (5) the waveforms *Id_t* and *Id_b* are presented. Figure 6 shows the dependencies of the losses *Pds_t* and *Pds_b* in the MOSFET transistors as a function of the current $I_{Lmax}$ for different junction temperatures. The macros described above are used and the *Append* function in the graphical analyzer *Probe* is applied.

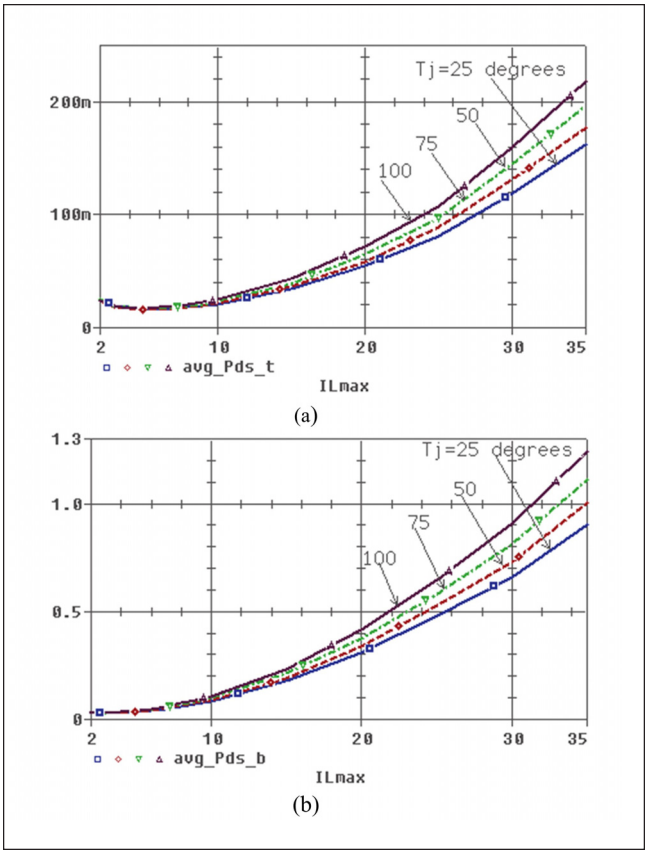


Figure 6. Dependences of MOSFET transistor losses in a function of *ILmax* for different junction temperatures: a) $P_{ds\text{-}t}$; b) $P_{ds\text{-}b}$

Figure 7 shows the dependency of BUCK converter efficiency as a function of the current $I_{Lmax}$ for different junction temperatures. Figure 8 shows the dependencies of the output power $P_{out}$; the output current $I_{out}$ and the average transistor currents: *Id_t* and *Id_b* as a function of the current $I_{Lmax}$.

## 4. Conclusion

The efficiency of BUCK DC-DC converter with ZVS has been studied. The scheme of the proposed Gate Driver allows obtaining of Adaptive Dead Time which ensures ZVS independently from the value of the switching current. The average values of the currents and the losses in transistors are simulated depending of the maximum value of the output current. The influence

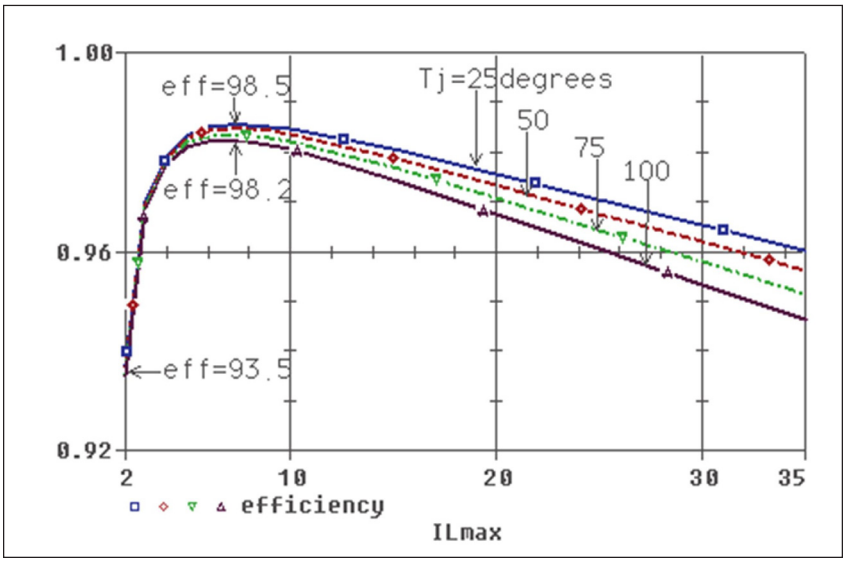


Figure 7. Current dependences of BUCK converter efficiency in a function of the junction temperature

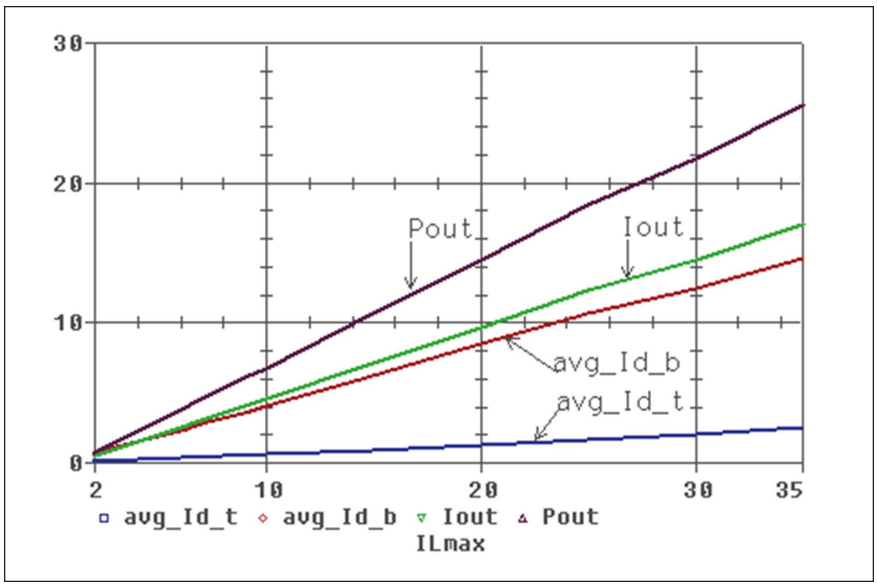


Figure 8. Dependence of: output power $P_{out}$; output current $I_{out}$ and average transistor currents *Id-t* and *Id-b*

of the additional drain-source connected capacitor on the Adaptive Dead Time, as well as on the peak value of the switching losses is investigated.

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